TM 11-7010-220-10-12

TECHNICAL MANUAL

OPERATION AND MAINTENANCE INSTRUCTIONS

DISCRETE DIGITAL INPUT/OUTPUT SUBSYSTEM
TYPE II
MODEL 3470-01
PART NUMBER 104059
AN/UYQ ( )

HEADQUARTERS, DEPARTMENT OF THE ARMY

NOVEMBER 1979

TM 11-7010-200-10-12

HEADQUARTERS
DEPARTMENT OF THE ARMY
Washington, DC, 30 November 1979

TM 11-7010-200-10-12, 30 November 1979, is published for the use of all concerned. This manual is a reprint of TO 31S5-4-523-1, 16 March 1978,

By Order of the Secretary of the Army

E. C. MEYER
General, United States Army
Chief of Staff

Official:

J. C. PENNINGTON
Major General, United States Army
The Adjutant General

DISTRIBUTION:
Active Army

TSG (1)
USAARENBD (1)
USAINSCOM (2)
TRADOC (2)
DARCOM (1)
TECOM (1)
OS Maj Comd (2)
USACC (2)
HISA (Ft Monmouth (21)
Armies (1)
USASIGS (10)
Svc Colleges (1)
WSMR (1)
USAERDAA (1)
USAERDAW (1)
Ft Richardson (CERCOM Ofc) (1)
Ft Carson (5)
Ft Gillem (5)

Army Dep (1) except
LBAD (10)
SAAD (10)
TOAD (14)
SHAD (3)
USA Dep (1)
Sig Sec USA Dep (1)
Units org under fol TOE:
29-134 (1)
29-136 (1)
29-207 (2)
29-610 (2)
Acct # MO497 (2)
" # DO741 (1)
" # HO534 (1)
" # AO049 (1)
" # SO392 (3)
" # JO861 (10)
" # CO214 (2)

NG: NONE

USAR: NONE

For explanation of abbreviations see, AR 310-50.

TABLE OF CONTENTS

CONTENTS (CONTINUED)

SECTION 3
OPERATING PROCEDURES

SECTION 4
INSTALLATION

CONTENTS (Continued)

CONTENTS (Continued)

APPENDICES

TABLES

CONTENTS (Continued)

ILLUSTRATIONS

SECTION 1
INTRODUCTION

1.1 PURPOSE

This technical manual provides information necessary to maintain a Discrete Digital Input/Output Subsystem Type 3 Model 3470-01, part number 104059.

1.2 SCOPE

The information given in this manual includes:

- Physical and functional descriptions of Hardwa
- Installation details.
- Operating procedures.
- Maintenance procedures.
- Reference information pertinent to field maintenance.
- Logic/Schematic diagrams.

The information in this manual is provided for use by a skilled technician familiar with standard test equipment, solid-state logic theory, common maintenance practices and standard troubleshooting techniques.

The scope of this manual is limited to the isolation of faults to the assembly level and correction of faults to the extent of replacing the assembly. Not covered in this manual are circuit board repair or system planning and engineering.

1.3 DOCUMENTATION

The following paragraphs define publications, drawings and conventions that support this manual.

1.3.1 Publications

The following publications support this field maintenance manual:

- A0003A IS/1000 Communications Processor Maintenance Manual
- B0037 IS/1000 Mechanical and Electrical Hardwa Maintenance Manual.
- E0006A IS/1000 Communications Processor User's Manual.
- H0011 IS/1000 I/O Interface Reference Manual.

1.3.2 Engineering Drawings

A complete set of logic/schematic diagrams for the DDIO Subsystem is included as part of this manual.

1.3.3 Abbreviations and Conventions

Abbreviations used in this publication are defined in Table 1-1. The following conventions are observed throughout the text:

- "$" preceding a number signifies that it is in hexadecimal notation.
- The names of instructions are capitalized for easy identification.
- Signal mnemonics that appear on logic diagrams and panel nomenclatures are reproduced in all upper-case characters.
- TELEPRINTER MESSAGES ARE REPRODUCED IN 1403 TYPE STYLE, AS SHOWN IN THIS EXAMPLE.
- Values represented in teleprinter messages by letters are reproduced in Scribe type style, as shown here.
- Signal polarity is indicated by a sign suffixed to the mnemonic. For example: PLXHFC- (negative signal), PLXHFC+ (positive signal).

Table 1-1. Abbreviations

Abbreviation	Meaning
A	Ampere.
ac	Alternating current.
CPU	Central processor unit.
DDIO	Discrete Digital Input/Output Subsystem.
DDIOB	Discrete Digital Input/Output Buffer.
DDIOC	Discrete Digital Input/Output Controller.
DIB	Data input bus.
DIG	Digital input group.
DOB	Data output bus.
DOG	Digital output group.
GTE/IS	General Telephone and Electronics Information Systems, Inc.
Hz	Hertz.
IC	Integrated circuit.
IDG	Input Driver Group.
I/O	Input/Output.
mA	Milliampere.
MHz	Megahertz.
ms	Milliseconds.
mV	Millivolts.
ns	Nanosecond.
ODG	Output Driver Group
OVP	Overvoltage protection.
PC	Printed circuit.
PCBA	Printed circuit board assembly.
us	Microsecond.
Vac	Volts, alternating current.
Vdc	Volts, direct current.

SECTION 2
DESCRIPTION

2.1 GENERAL

The DDIO Subsystem is designed to provide an Input/Output interface between an IS/1000 Communications Processor and external user data or control lines. A typical DDIO Subsystem installation is illustrated in Figure 2-1.

Presented in this section are physical and functional descriptions of the DDIO Subsystem. Included are physical descriptions of all assemblies, basic block diagrams with accompanying major block descriptions, and detailed functional descriptions of the major components of the DDIO Subsystem.

2.2 PHYSICAL DESCRIPTION

DDIO Subsystem components are listed in Table 2-1. These components are physically described in the following paragraphs.

2.2.1 DDIO Controller

The DDIO Controller (DDIOC) is packaged on a standard PC board designed to mount horizontally in the IS/1000 Communications Processor chassis (Figure 2-2). The DDIOC has connectors J1 and J2 on the front edge for I/O bus plugs, and connectors J11 and J12 at the rear for twisted wire plugs.

2.2.2 DDIO Buffer Group

The DDIO Buffer (DDIOB) group is comprised of the following assemblies:

2.2.2.1 Card File Assembly

The DDIO Card File assembly (Figure 2-3) provides the physical support and power and signal connections for the various DDIO PC boards.

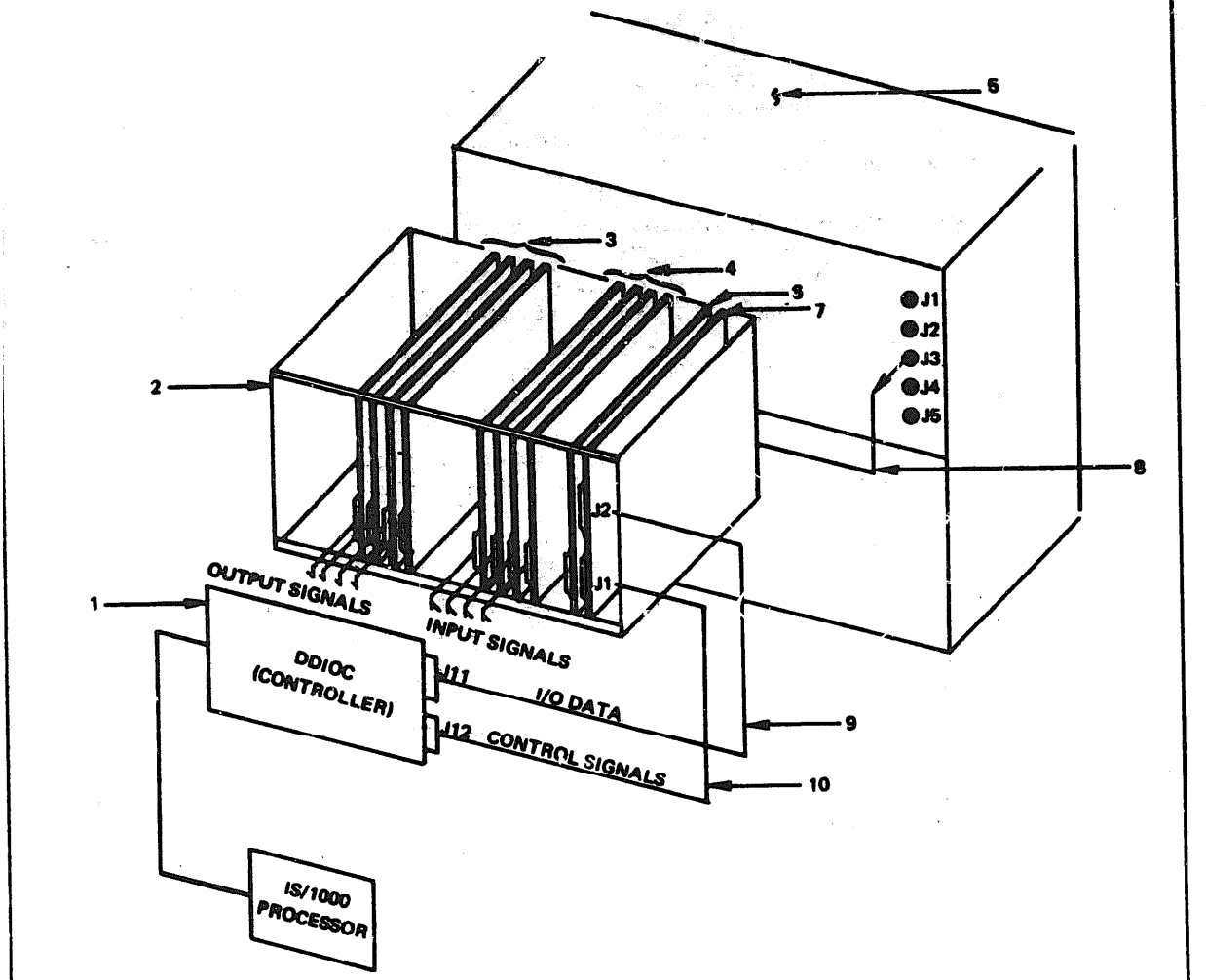
The card file has a back panel containing 10, 80-pin, PC board connectors.

The back panel has signal interconnections and conductors to distribute +5-, +12-, and -12-Vdc power to all boards. A ground plane is also provided to all PC boards.

The PC boards housed in the DDIO Card File Assembly are physically described in the following paragraphs.

2.2.2.2 Transceiver/Decoder PCBA

The Transceiver/Decoder PCBA (Figure 2-4) has two connectors (J1 and J2) on the front edge of the board which interface with the DDIO



1. DDIO PCBA, 104036
2. CARD FILE ASSY, 104060
3. DIGITAL OUTPUT GROUP PCBAs, 104048
4. DIGITAL INPUT GROUP PCBAs, 104040
5. COMMUNICATIONS POWER SUPPLY, 101531
6. BUS TERMINATOR ASSY, 101520
7. TRANSCEIVER/DECODER PCBA, 104050
8. POWER CABLE ASSY, 101596
9. DATA CABLE ASSY, 104199
10. CONTROL CABLE ASSY, 104198

I1144

Figure 2-1. Typical DDIO Subsystem

Table 2-1. DDIO Subsystem Components

Quantity	Description	Part Number
1	DDIO Controller	104036
1	Communications Power Supply*	101531
	Buffer group comprised of:	
1	Card File Assembly	104060
1	Transceiver/Decoder PCBA	104050
16 max.**	Digital Input Receiver PCBA	104040
16 max.**	Digital Output Driver PCBA	104048
1	Bus Terminator Assembly	101520
	Bus Extender Assembly (Optional)	101521
1	Power Cable Assembly	101596
1	Data Cable Assembly	104199
1	Control Cable Assembly	104198
1	Test Cable Assembly	

*Coverage supplied in GTE/IS manual B0037.
**Refer to System Configuration Specification for type and quantity of PC boards.

controller. Connector P1 at the rear of the Transceiver/Decoder board plugs into the card file backplane to interface w Digital Input and Digital Output PCBAs.

2.2.2.3 Digital Input PCBA

The Digital Input PCBA (Figure 2-5) has a connector (J1) on the front edge of the board through which input signals are received from an external user device. Connector P1 at the rear of the board plugs into the card file backplane to interface with the Transceiver/ Decoder PCBA.

2.2.2.4 Digital Output PCBA

The Digital Output PCBA (Figure 2-6) has a connector (J1) on the front edge of the board through which output signals are transmitted to an external user device. Connector P1 at the rear of the board plugs into the card file backplane to interface with the Transceiver/ Decoder PCBA.

2.2.2.5 Bus Terminator assembly

The Bus Terminator Assembly board (Figure 2-7) provides a termination for the controller bus through connector P1.

2.2.2.6 Bus Extender assembly

The optional Bus Extender Assembly (Figure 2-8) is utilized, when more than 16 input or output boards are required, to provide interface between two card files.

2.2.2.7 Cable Assembly

DDIO Subsystem cable assemblies are illustrated in Figure 2-9.

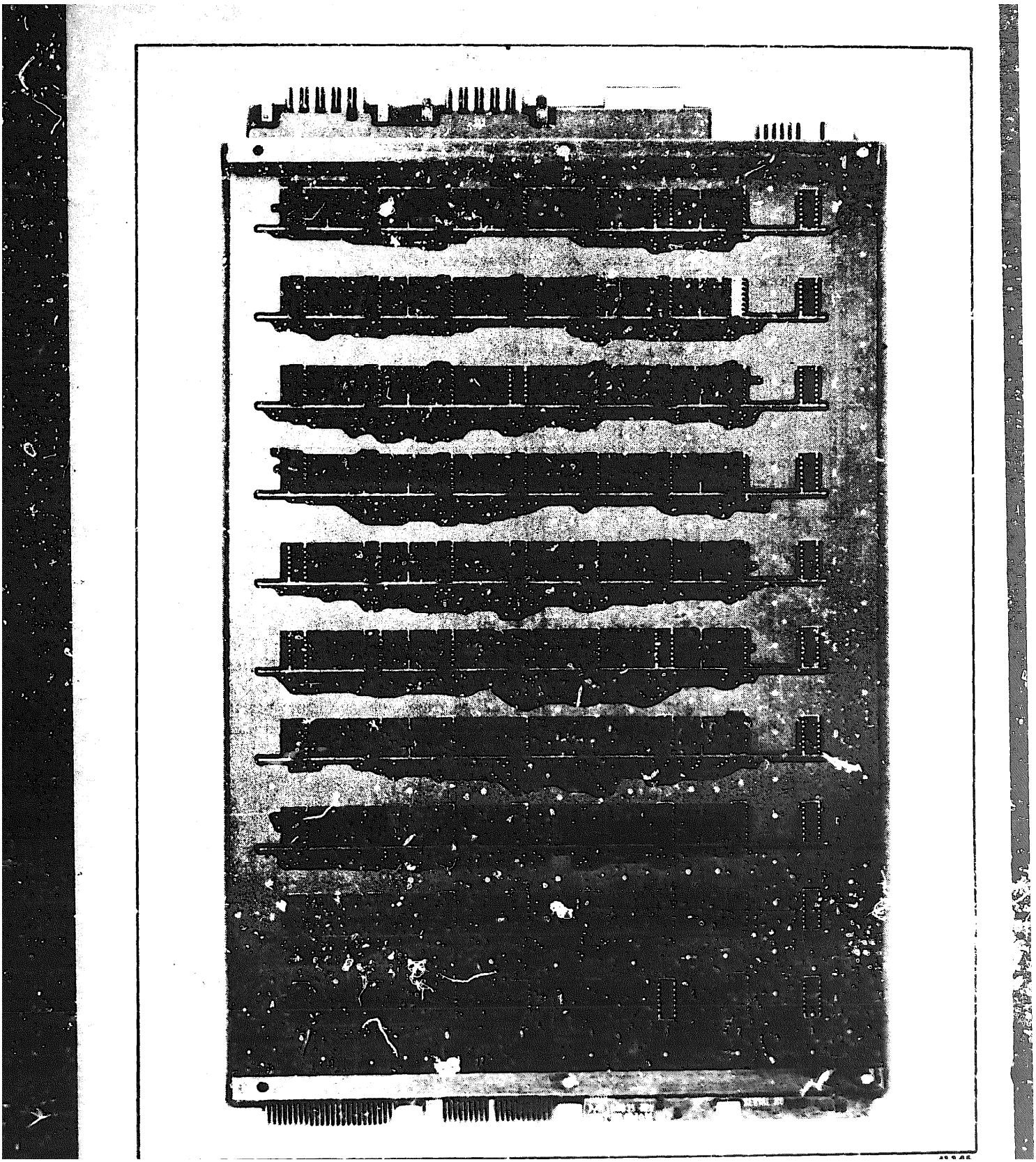
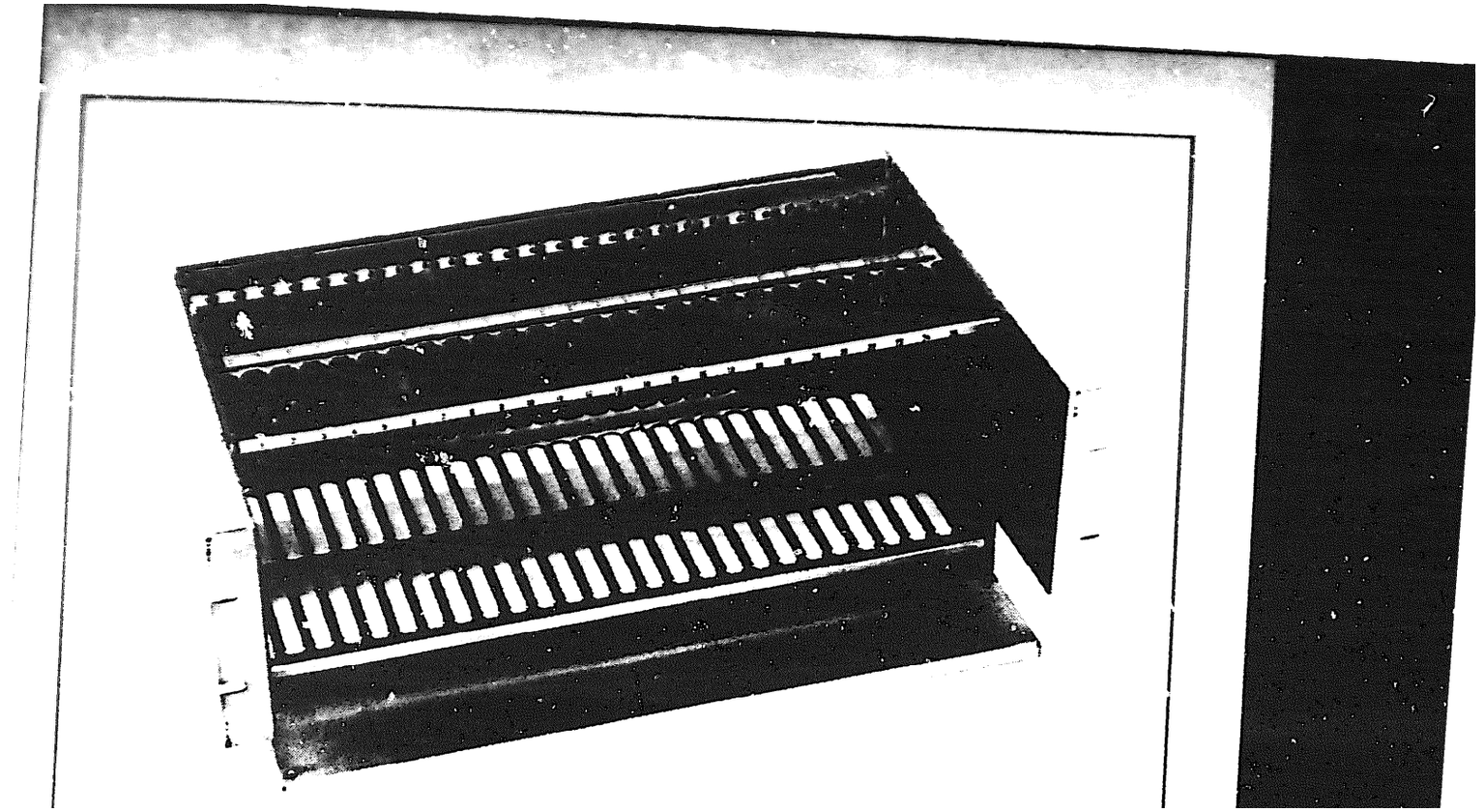
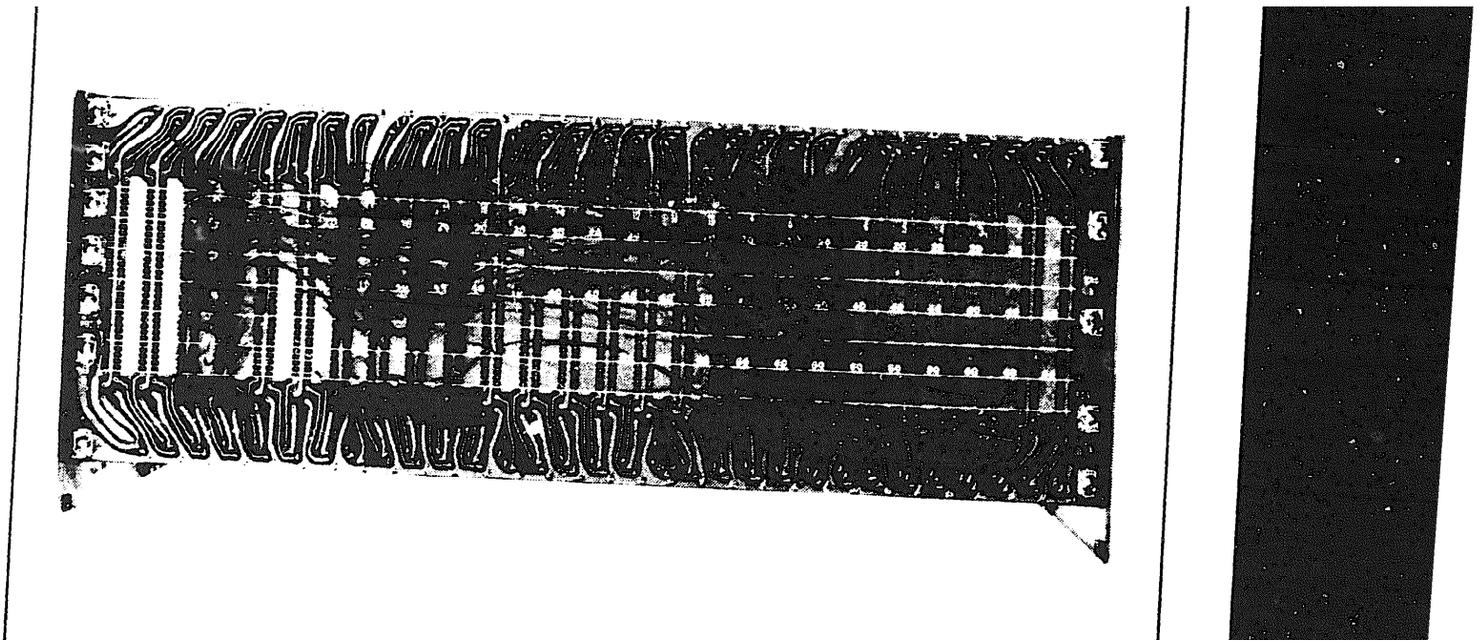


Figure 2-2. DDIO Controller PCBA



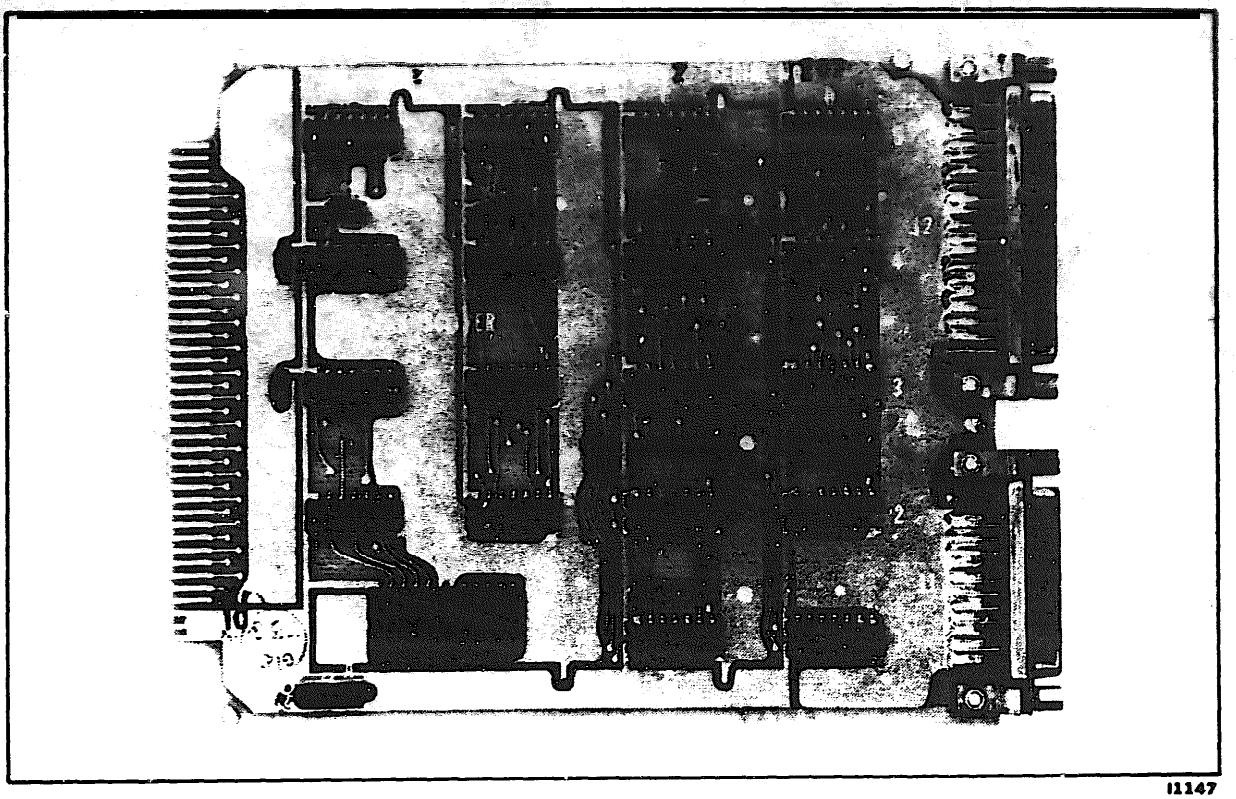
FRONT



REAR

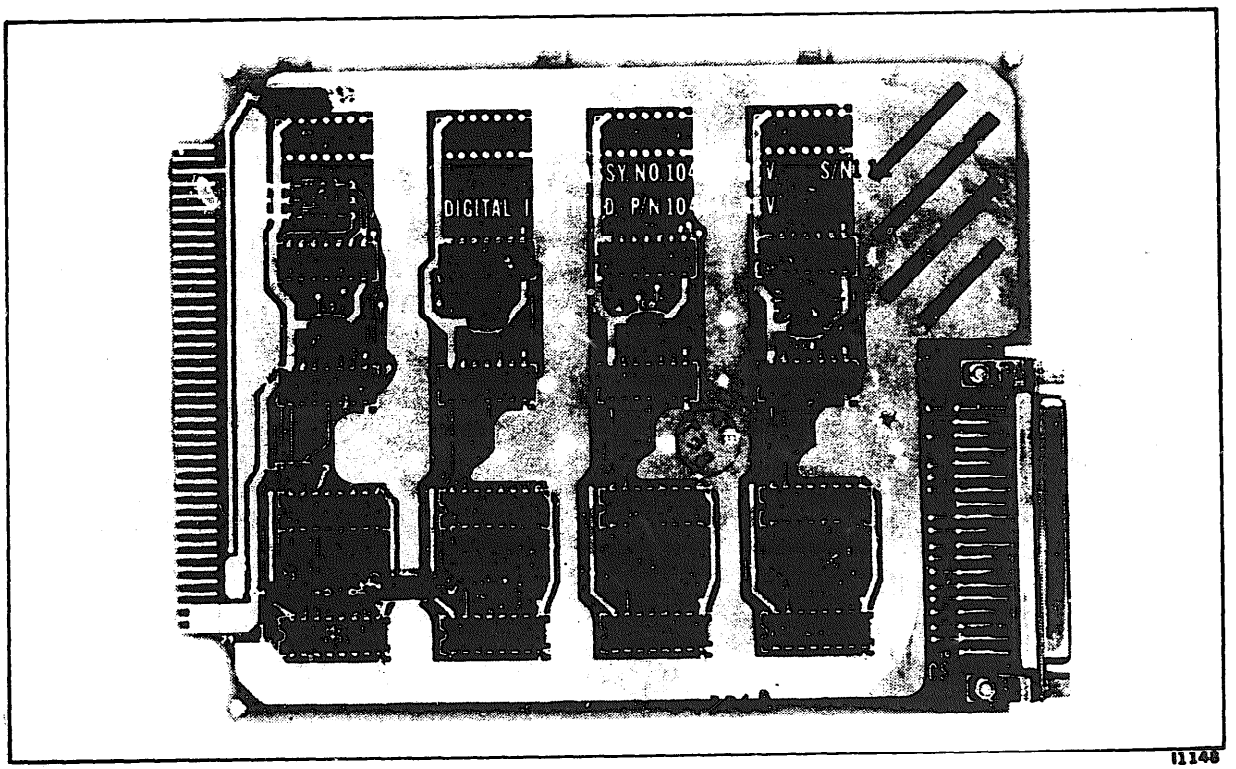
Figure 2-3. DDIO Card File Assembly

11146



I1147

Figure 2-4. Transceiver/Decoder PCBA



I1148

Figure 2-5. Digital Input PCBA

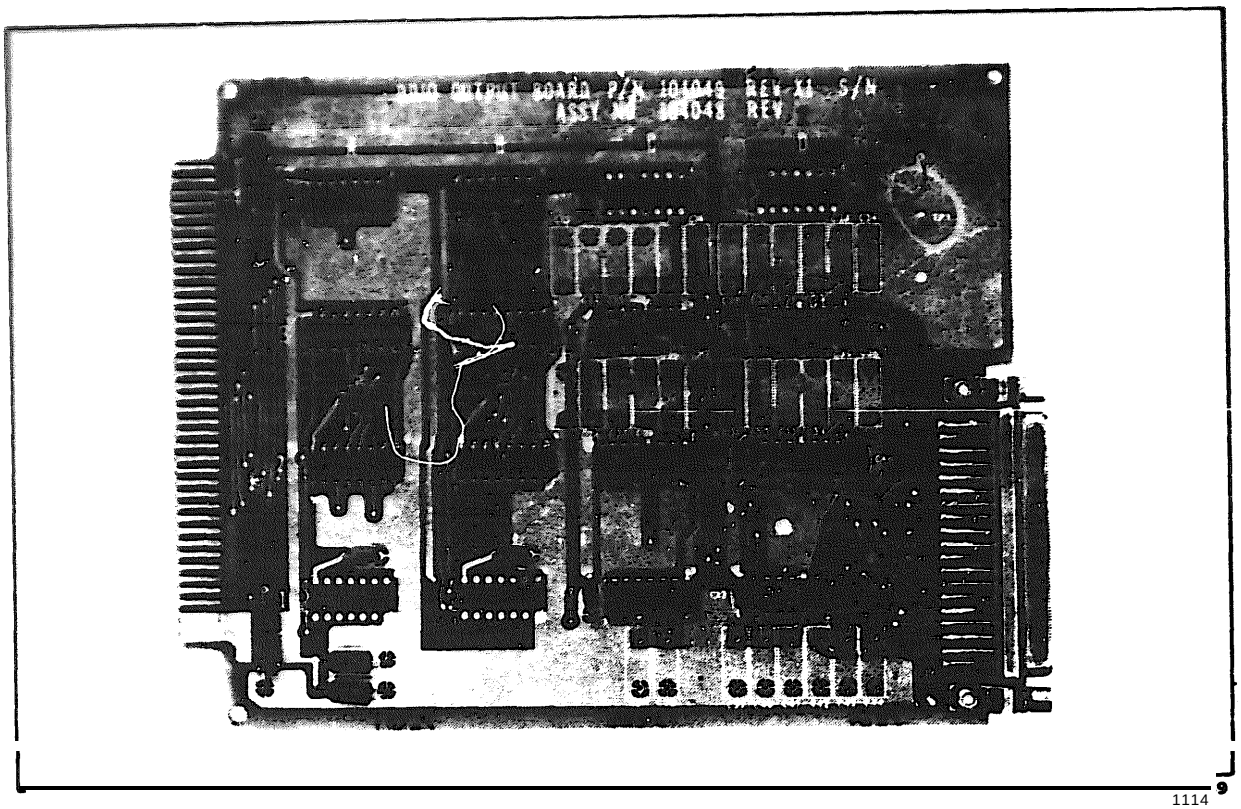


Figure *2-6.* Digital Output PCBA

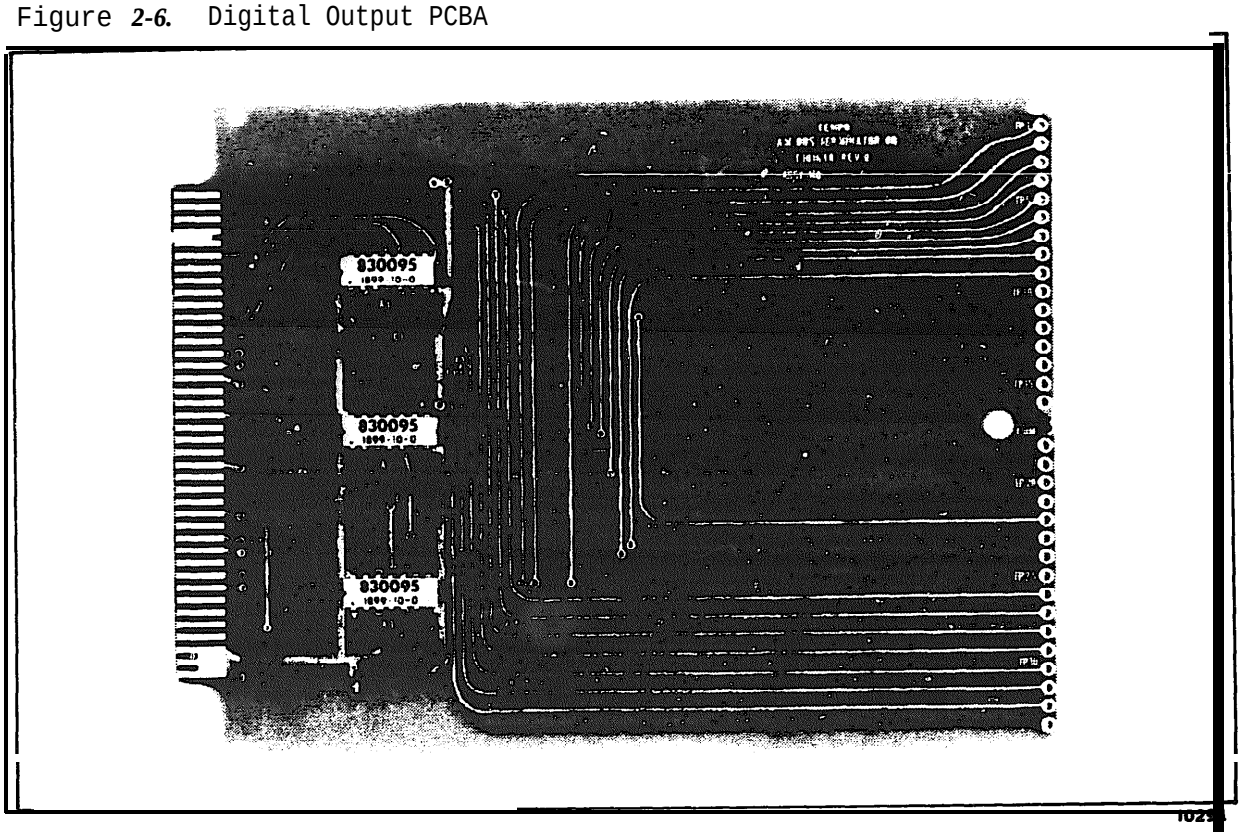
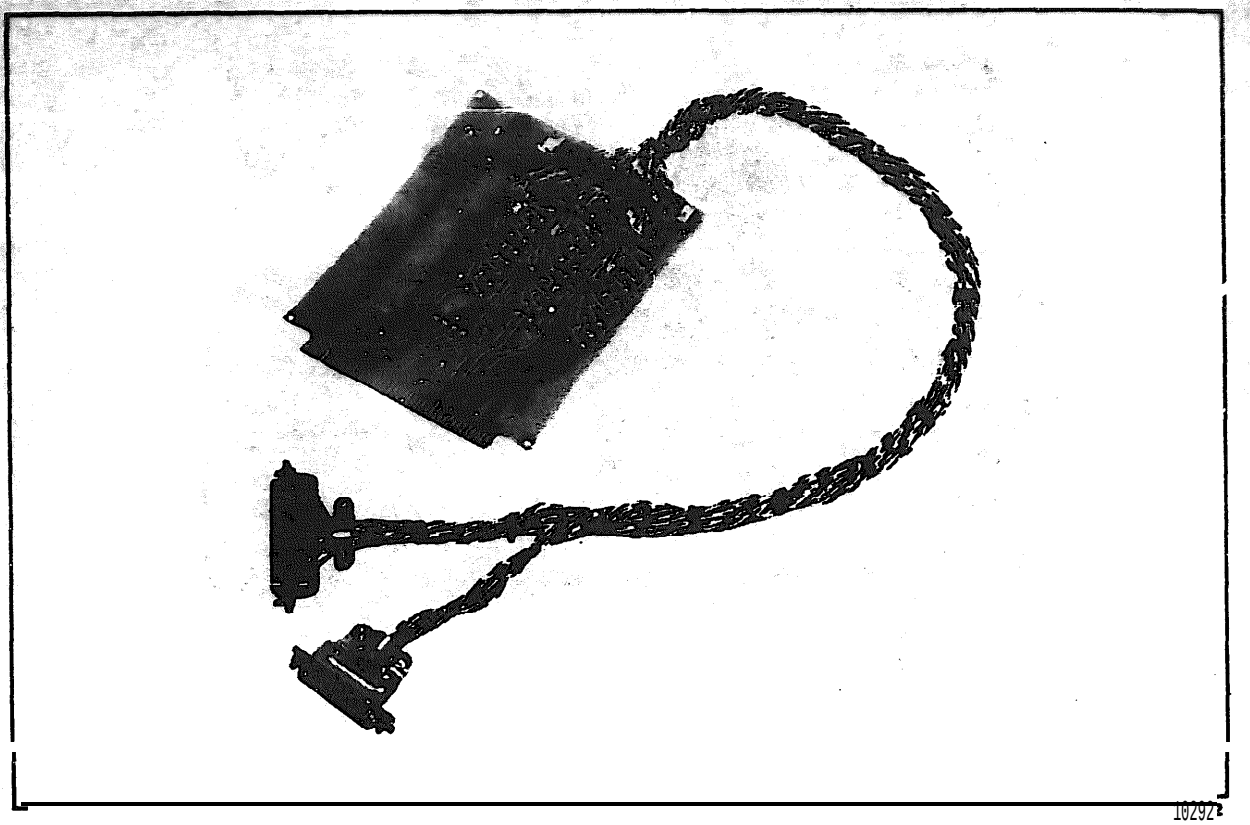
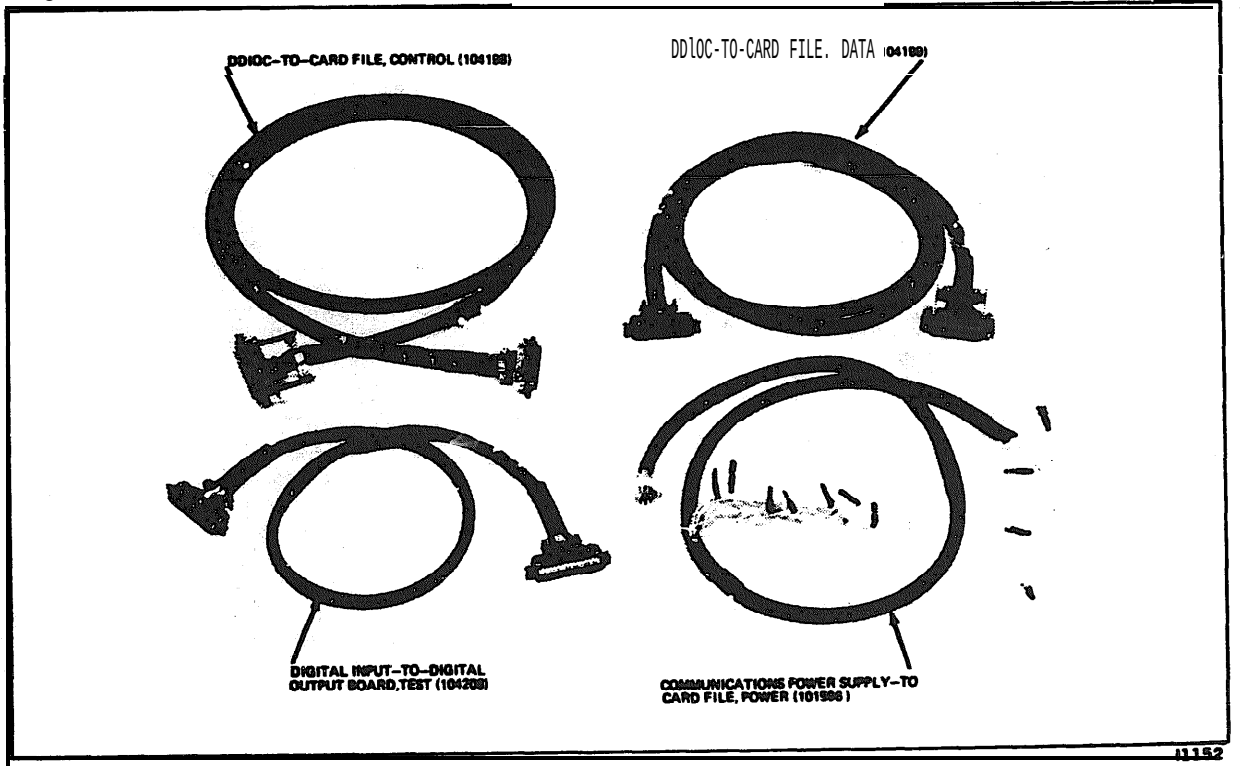


Figure 2-7. Bus Terminator Board



10292

Figure 2-8. Bus Extender Assembly (Optional)



11152

Figure 2-9. DDIO Cable Assemblies

Figure 2-10 provides a simplified overall block diagram of the DDIO Subsystem. These functional blocks are briefly described in this paragraph.

The DDIO Subsystem is comprised of the Discrete Digital Input/Output Controller (DDIOC) and Discrete Digital Input/Output Buffer (DDIOB) group. The DDIO Subsystem provides an interface between the GTE/IS IS/1000 Communications Processor and external user devices.

The DDIOC assembly provides command control, group address, I/O data, sequence control, and interrupt control between the processor and DDIOB.

Signal compatibility and distribution of data to and from 32 user device lines (typical configuration presented in this manual) is performed by the DDIOB under control of the DDIOC. Additional assemblies can extend the interface capacity to 256 device input/output data lines. These lines are addressed in input/output groups of sixteen.

The DDIO Subsystem operates in a half-duplex mode, providing either data input or output through a bi-directional I/O bus. Sixteen input or output lines (per board) form a group. One input/output group is selected at a time. Data may be repetitively processed sequentially from one group or randomly, under processor control, from more than one group.

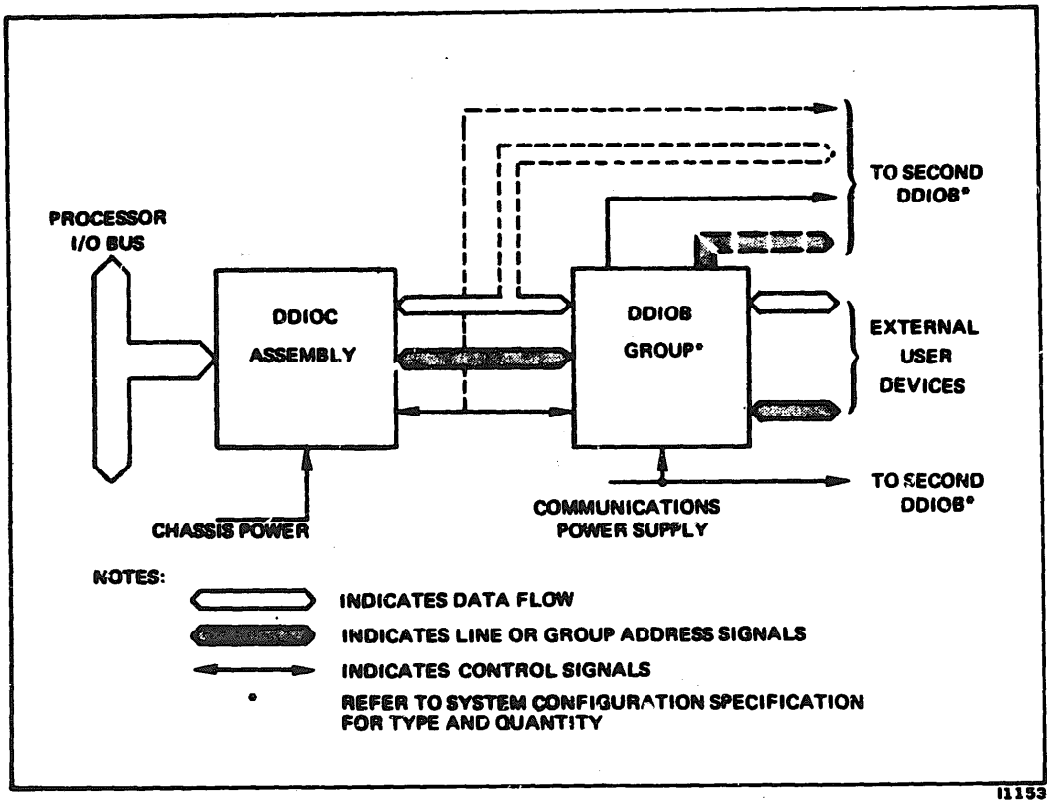


Figure 2-10. DDIO Subsystem Simplified Block Diagram

Inherently, the data transfer rate between a processor and the DDIO is 800,000 words per second. When used with the IS/1000, the data transfer rate is 77,000 words per second.

2.3.1 Functional Blocks

Figure 2-11 is a detailed functional block diagram of the DDIO Subsystem. It depicts the major functional logic groups of the DDIOC and DDIOB. Major data, address, and control signal paths between the processor, major logic groups, and the external devices are shown. Each block is functionally described in the following paragraphs and is keyed to its respective logic diagram in Appendix D.

2.3.1.1 DDIOC Assembly

The following functions are performed by the DDIOC Assembly:

- Sequencing control of I/O data and control signals between the processor and DDIOB.
- Data, control, and address signal level gain.
- Program interrupt processing between the DDIOB and processor.

2.3.1.1.1 Control Drivers/Receivers. Control signals to and from the processor, via the I/O bus, are maintained at optimum characteristics by the Control Drivers/Receivers.

2.3.1.1.2 Command Decode Logic. All functions within the DDIOC are controlled by decoding the control signals from the control drivers/receivers. Address recognition, command decode, and interrupt logic are some of these functions.

Manually alterable address patches respond to the wired-in address preassigned to the controller.

One decoded address signal is used to sequence the transfer of input or output data. Provision is included, although, for separate addressing of input or output data transfer. The simultaneous decoded address signals are ADDA- and ADDB-.

Command decode of EDF-, WTO-, WTI-, RDS-, OOS-, OF7-, and ICI- signa is provided by this logic. Combining these various terms with eithe ADDA- or ADDB- enables either input or output data transfer.

2.3.1.1.3 Sequence Control Logic. The sequence control logic receives decoded command signals from the command decode logic. The commands are applied to three counters as follows:

WTICMD - Word Transfer in counter

WTOCMD - Word transfer out counter

CIA/B
OOS
RDSCMD
} Command sequence counter

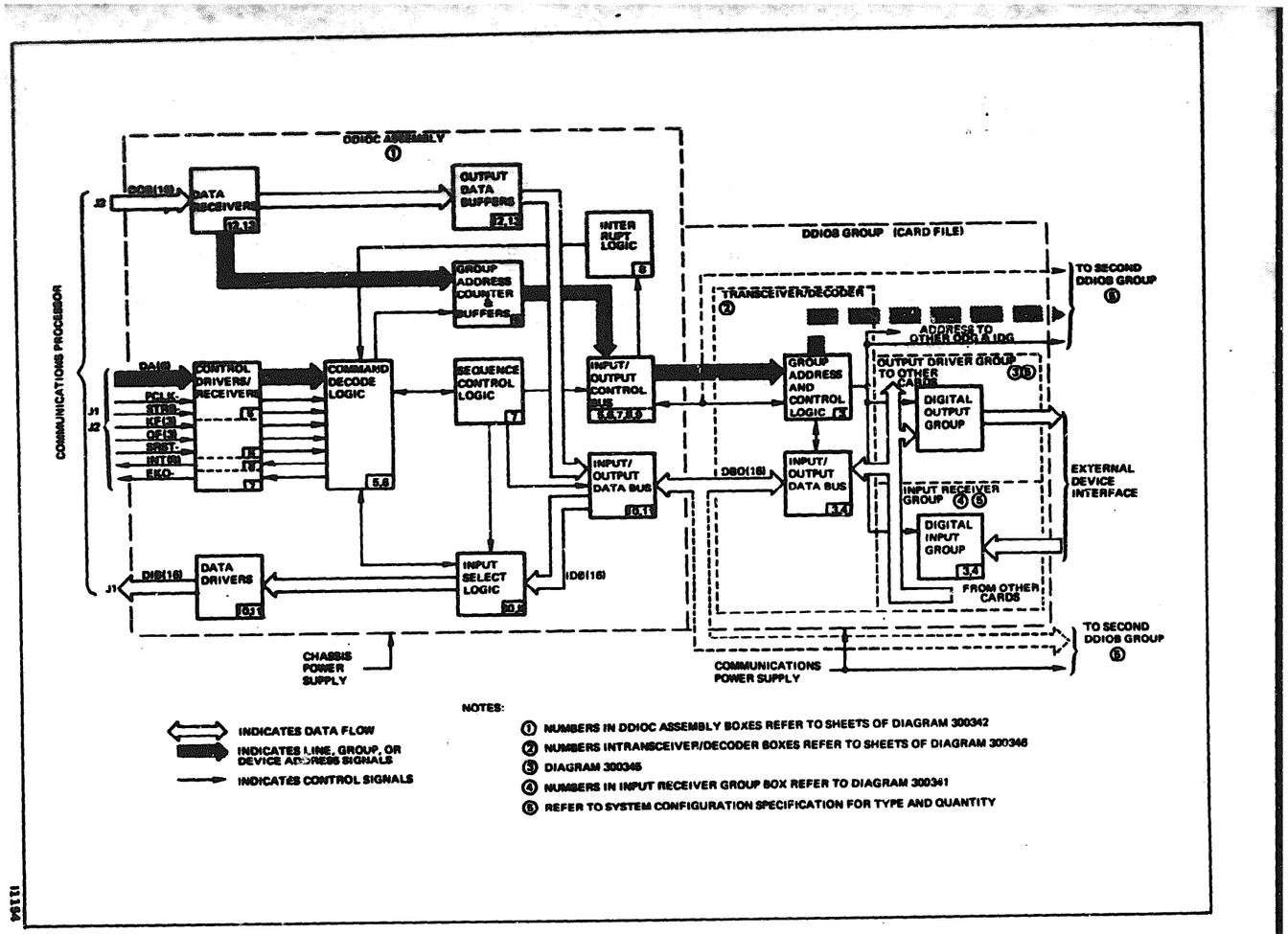


Figure 2-11. DDIO Subsystem Detailed Functional Block Diagram.

Each counter cycles through four sequence states upon command. These states are:

State	F/F Count MSB	LSB
0	0	0
1	0	1
2	1	1
3	1	0

Each sequence counter is initiated by a decoded address of the controller, as described under Command Decode Logic.

If the command is a word transfer out (WTO), the WTO counter will initiate a data output sequence from the processor. The timing waveforms for the WTO are shown in Figure 2-12. At sequence time OSEQ1, processor data is entered into the output data buffers. Signal EKO- is sent to the processor during OSEQ2- time. At the end of OSEQ2 time, the data is transferred to the DDIOB. If WTOIEN+ is true, the group address counter is incremented at OSEQ3 time.

A decoded word transfer in command (WTI) initiates a data input sequence to the processor. Data is gated to the processor and the sequence counter advances to ISEQ1. At advance to ISEQ2 time, EKO- is produced. If WTIIEN+ is true, the group address counter is incremented at ISEQ3 time.

If common interrupt A or B (CIA- or CIB-), EDF one or seven (OOS-), read intermediate register (OF7-), or request controller status (RDS) is received, the command sequence counter will advance to the sequence one state while responding to the command. When the action is complete, and the counter advances to state two, an EKO is returned to the processor. State two is entered and maintained until the command is dropped by the processor. The counter then advances to state three and then zero.

2.3.1.1.4 Data Receivers. Sixteen parallel discrete data signals from the processor (DOB00- to DOB15-) are applied to sixteen line receivers. The receivers maintain the signals at their optimum characteristics. The 16 received data signals are then applied to the output data buffer.

2.3.1.1.5 Output Data Buffers The 16 possible data signals are temporarily stored in the output data buffer registers. An output data sequence one control signal (OSEQ1-) transfers data into the buffer registers. A sequence state two (OSEQA+) transfers the register's contents to 16 I/O data bus line drivers (DB00 to DB15), for transmission to the DDIOB. Signal gain is also provided to optimize data transfer to that unit.

2.3.1.1.6 Input/Output Data Bus. The bi-directional input/output data bus comprises 16 wire paths between the DDIOC and DDIOB. Input data is available for transfer unless an output data request is

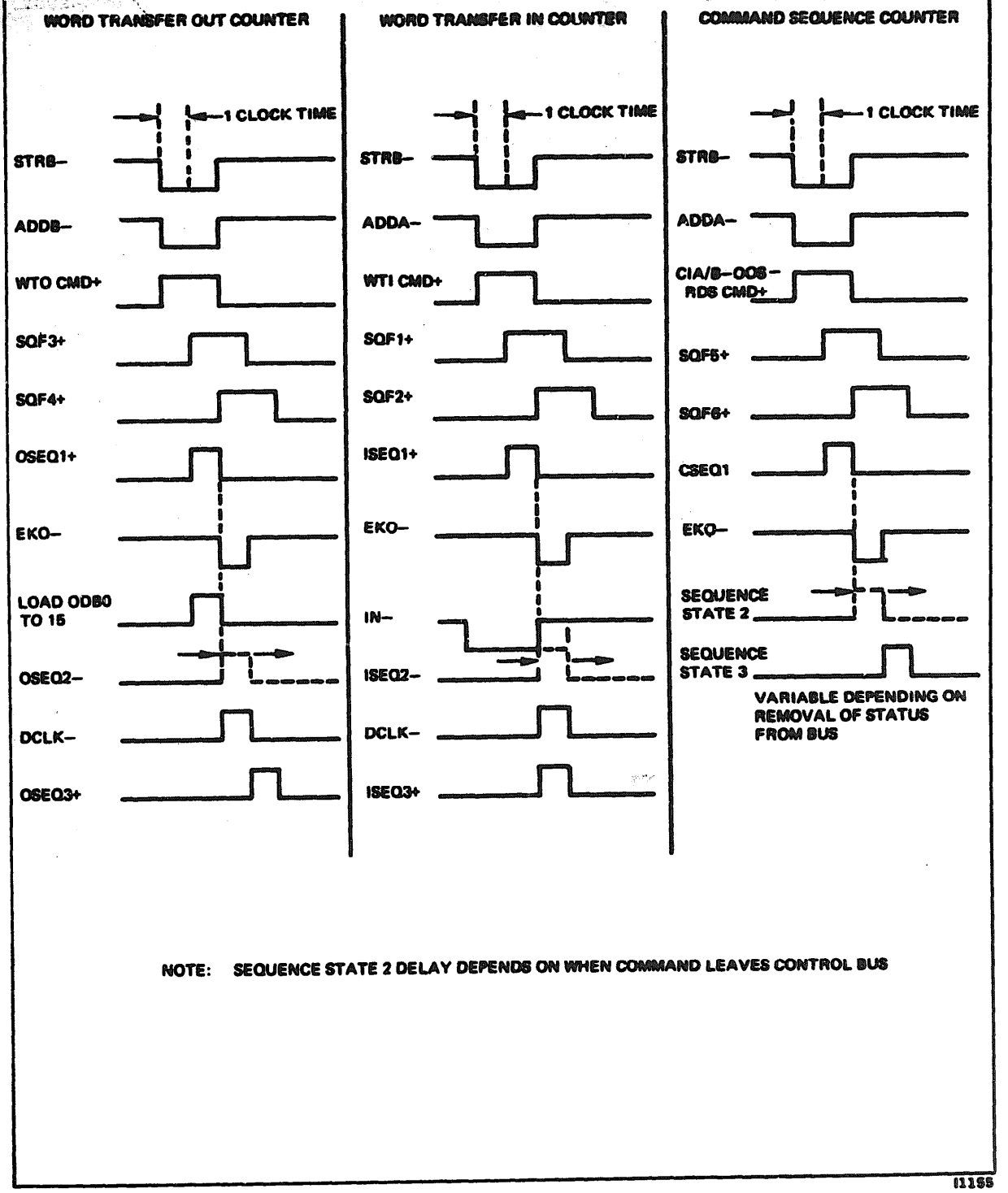


Figure 2-12. Sequence Control Waveforms

made. Each data bus line DB00- thru DB15- is terminated with an equivalent 120 ohms impedance to match the bus characteristics.

2.3.1.1.7 Input selection Logic. Either data from the DDIOB or controller functional status are selected for transfer to the processor. The status information is:

- Interrupt (input/output).
- Group select number.
- Word transfer increment enable (WTOIEN/WTIIEN).
- Interrupt enable (input/output).

2.3.1.1.8 Data Drivers. Sixteen parallel discrete data signals from the input select logic are applied to sixteen line drivers. Signal gain is provided to optimize data transfer to the processor.

2.3.1.1.9 Group Address Counter and Buffers. A maximum of 16 DDIOBs can be accommodated by each DDIOC. Selection of the DDIOBs is performed by the address counter. This selection is either forced by bits 12 thru 15 of the EDF command word (EDF CWD) or incremeted by a decoded command. The decoded commands increment the counter by binary count of one. During OSEQ3+ if WTOIEN+ is true, or during ISEQ3+ if WTIIEN+ is true, the counter will advance.

Four selection lines from the counter are buffered and applied to the input/output control bus and input/output select logic (for RDS command). Text lists the device lines that correspond to the group selected.

Table 2-2. Group/User Device Line Selection

Group	Lines Selected
0	0 - 15
1	16 - 31
2	32 - 47
3	48 - 63
4	64 - 79
5	80 - 95
6	96 - 111
7	112 - 127
8	128 - 143
9	144 - 159
10	160 - 175
11	176 - 191
12	192 - 207
13	208 - 223
14	224 - 239
15	240 - 255
Note: Groups 2 thru 15 are not presently implemented	

2.3.1.1.10 Input/Output Control Bus. The control signals between the DDIOC and DDIOB are transferred over the Input/Output Control Bus. The following control signals are sent to the DDIOB:

- Group address (GSC0- to GSC3-).
- Input sequences (ISEQA-).
- Reset (RST-).
- Data Clock (DCLK-).
- Output select (OUT-).

Control signals from the DDIOB to the DDIOC are:

- External interrupt (EII- and EOI-).

Each bus line is terminated in an equivalent impendance of 120 ohms.

2.3.1.1.11 Interrupt Logic. The controller, when producing an interrupt signal, has its priority and address processed by the interrupt logic for entry into the processor. Patches are provided to change the priority level.

A direct interrupt line assignment is made through a patch. For common interrupt lines, an interrogate common interrupt command (ICICMDA) results in a response through a patch to indicate which one controller out of sixteen produced the interrupt. The assignment level is interpreted by the processor as an interrupt priority level.

2.3.1.2 DDIOB Group

The following functions are performed by the DDIOB group:

- External device signal compatibility.
- Address decoding for each of a maximum of 256 user device lines addressed in 16 groups of 16 lines each (32 lines are used in this manual as an example).

A DDIOB group is comprised of a transceiver/decoder, an output driver group (ODG) and an input driver group (IDG). The components for each of these three major functions are mounted on separate PC cards. Each of these functions are described in the following paragraphs. The five cards, comprising the typical DDIOB installation described, require the following power:

+12 Vdc 390 ma

-12 Vdc 340 ma

+5 Vdc 2.28A

2.3.1.2.1 Transceiver/Decoder. The transceiver/decoder transfers data and control signals between the DDIOB and DDIOC.

The group address and control logic decodes the group address signals, GSC0- to GSC3-, produced by the controller group address counter and buffers. The first eight ODGs and IDGs are addressed by one DDIOB. Groups 9 thru 15 are addressed by the other DDIOB. (Other address groupings are available when requested from the manufacturer.) Each ODG and IDG is composed of 16 drivers and receivers respectively. Data clock (DCLK+) and reset (RST+) signals are conditioned and routed, to the output driver storage registers. Input and output interrupt signals (EII- and EOI-) are transferred to the controller from the using device over the control bus.

Data is transferred over 16 bi-directional bus lines in the I/0 data bus. Data transfer is controlled by I/O sequence signals. Each bus line is terminated in 120 ohms.

2.3.1.2.2 Output Drivers Group. Output data signals to the using devices are produced by 16 output line drivers. *Temporary* storage registers receive the controller date. The output data transfer is synchronized by the data clock (DCIK-1) pulse. Output data transfer takes place at the end of output counter state OSEQ2. Each of the two cards comprising the output driver group requires the following power:

+12-Vdc 90 ma

-12-Vdc 90 ma

+5-Vdc 260 ma

2.3.1.2.3 Input Driver Group. Input data signals applied to the I/O data bus are converted to TTL compatible signals by 16 input line receivers. Data transfer is *under* control of input signal LDA+. User device interrupt signals, PINT1- to PINT6- are processed and result in common interrupt signal CI-.

Each card of the input driver group *requires* the following power:

+12V 0.108A

-12V 0.084A

+5V 0.328A

2.3.1.3 Additional DDIOB Group

When more than 16 input/output driver boards are required, a second card file must be added. This necessitates the removal of the terminator board, and its replacement with an optional bus extender board. The terminator board is used in the second card file.

The bus extender board provides paths for the data, address, and control signals. The line terminations are moved to the second card file for proper line impedance matching.

2.3.1.4 Data Input/Output Transfer Path

Figure 2-13 depicts the data path between the processor and user device for bit DOB00.

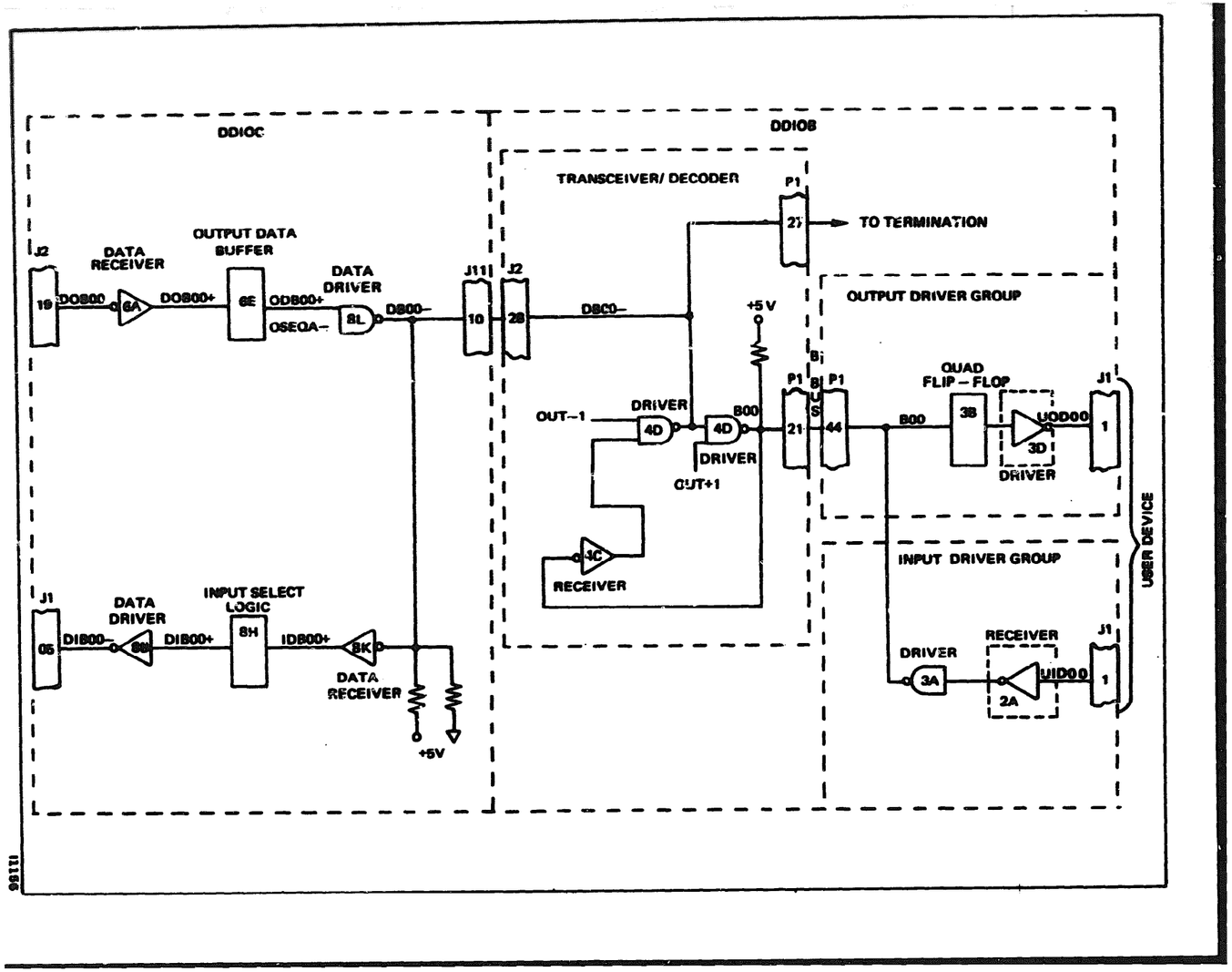


Figure 2-13. Data Input/Output Transfer Path

The output path from the processor to the user device functions as follows: The data bit is received by the controller (6A), processed, and applied to the buffer transceiver/decoder driver (4D). For transmission, the bit is gated through 4D by OUT+1. Normally, when not transmitting, data is being received and gated by OUT-1 being true. When transmitting, the B-bus is positive true. At all other times it is negative true. The output data bit is then processed by the buffer output driver flip-flop (3B) and driven by driver (3D).

The input data bit path functions as follows: The buffer input receiver (2A) and driver (3A) drive the B bus. The negative true signal is applied to buffer transceiver/decoder receiver (4C). It is gated through driver (4D) and applied to data receiver (8K). After being processed by input select logic (8H), data driver (8B) transmits the data bit to the processor.

Figure 2-14 shows the overall input/output timing for the DDIOC. Waveform OUT+ goes true with OSEQ1+, and false with OSEQ3+. Card file clock DCLK+ is bracketed by OUT+. B-bus coincides with OUT+, and is shown true during transmission.

2.3.2 Software

The following paragraphs provide software information for the DDIO Subsystem.

2.3.2.1 Device Address

The DDIOC responds to one plugboard selectable device address and has one interrupt that also is plugboard selectable. The interrupt can be commoned with other device interrupts. Commoned interrupts are identified through the use of ICI. Interrupt priority and ICI response are plugboard selectable.

2.3.2.2 Instruction Set

The following I/O instructions are accepted by the DDIO Subsystem hardware:

Mnemonic	Name
EDF RST	Program Reset.
EDF CWD	Command Word.
WTO	Word Transfer Out.
WTI	Word Transfer In.
WTI7	Read Intermediate Register.
RDS	Request Device Status.
ICI	Interrogate Common Interrupts.

A brief description of each DDIO Subsystem instruction is provided in the following paragraphs (machine language formats for DDIO Subsystem instructions are given in Appendix A). Each of the DDIO Subsystem

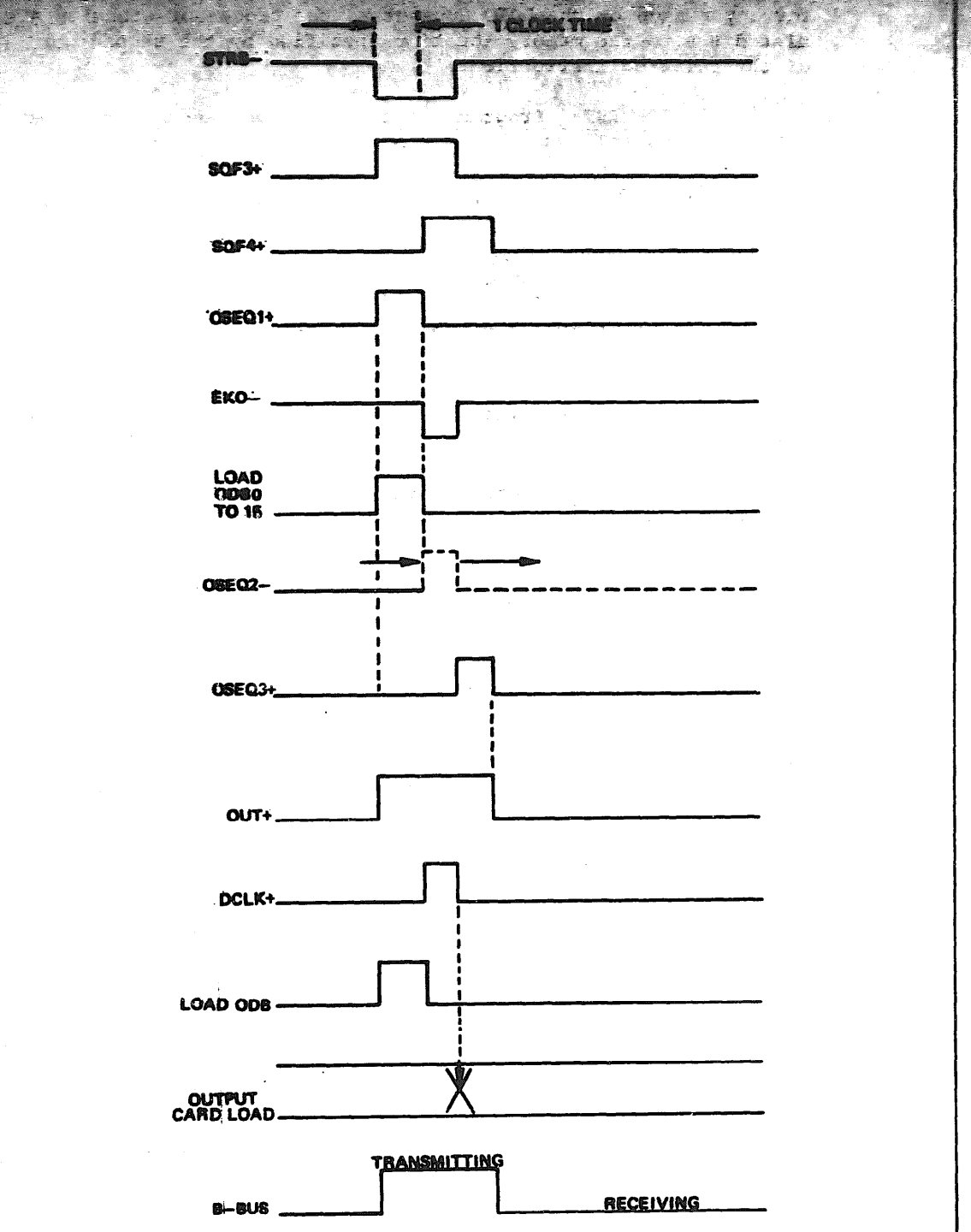


Figure 2-14. Data Input/Output Timing Diagram

instructions is composed of two-words. If an instruction is rejected for any reason by the DDIO Subsystem, the processor executes a simulated BSP to the memory location specified by the second word (Y) of the rejected instruction.

2.3.2.2.1 EDF RST: Program Reset The Macro Assembler format for EDF RST is as follows:

```
EDF D,Y,7
```

where:

D = device address.

Y = address of branch on reject of instruction.

7 = order line code.

EDF RST resets all control logic, input driver groups, and output driver groups.

2.3.2.2.2 EDF CWD: Command Word.
EDF CWD is as follows:

```
EDF D,Y,1
```

where:

D = device address.

Y = address of branch on reject of instruction.

1 = order line code.

EDF CWD supplies all command information to the DDIO Subsystem.

2.3.2.2.3 WTO: Word Transfer Out. The Macro Assembler format for WTO is as follows:

```
WTO D,Y
```

Where:

D = device address.

Y = address of branch on reject of instruction.

WTO transfers data from the processor A-Register to the data output cards via the intermediate register.

2.3.2.2.4 WTI: Word Transfer In The Macro Assembler format for WTI is as follows:

```
WTI D,Y,0-6
```

where:

D = device address.

Y = address of branch on reject of instruction.

0-6 = order line codes.

WTI reads data from the data input cards into the A-Register.

2.3.2.2.5 WTI7: Read Intermediate Register. The Macro Assembler format for WTI7 is as follows:

```
WTI D,Y,7
```

where:

D = device address.

Y = address of branch on reject of instruction.

7 = order line code.

WTI7 reads the contents of the intermediate register into the A-Register.

2.3.2.2.6 RDS: Request Device Status. The Macro Assembler format for RDS is as follows:

```
RDS D,Y
```

where:

D = device address.

Y = address of branch on reject of instruction.

RDS causes the DDIO status word (Figure 2-15) to be transferred to the processor. This instruction is issued in response to an interrupt initiated by the DDIO.

2.3.2.2.7 ICI: Interrogate Common Interrupts. The Macro Assembler format for ICI is as follows:

```
ICI D,Y
```

where:

D = device address.

Y = address of branch on reject of instruction.

ICI causes a plugboard selected data input line to the processor to be true if the DDIO has sent a common interrupt request. ICI is rejected if the DDIO common interrupt is not enabled or an interrupt request has not been initiated by the DDIO.

2.3.2.3 Word Format

Receipt of an RDS command results in acquiring the DDIOC status shown in Figure 2-15. When an EDF command (O field-1) is received by the DDIOC, the A-register contents shown in Figure 2-16 are received and acted upon by the DDIOC.

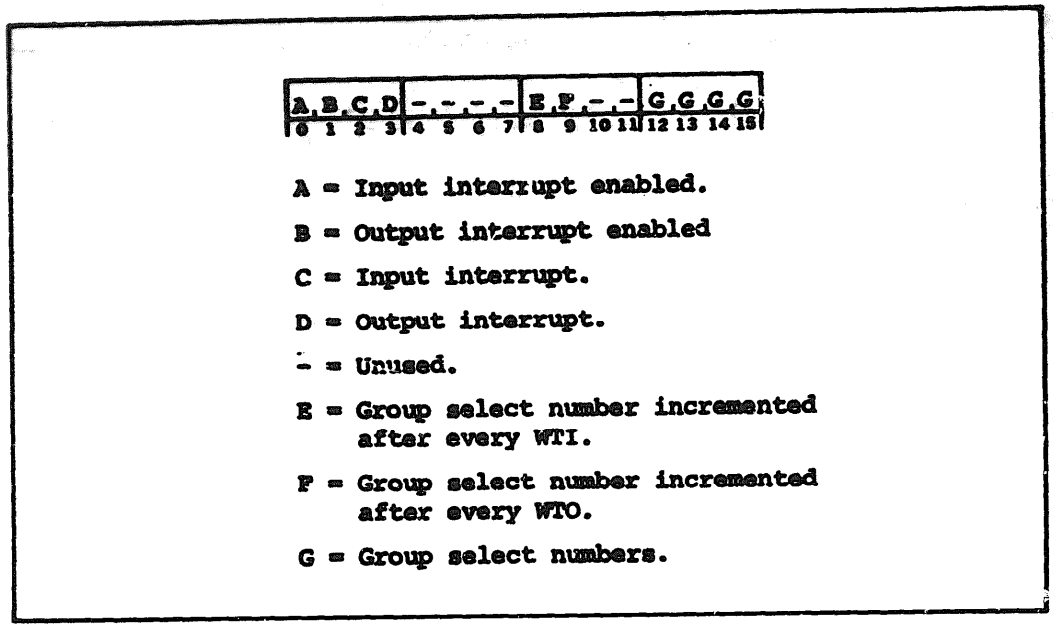


Figure 2-15. DDIOC Status Word Format for RDS Command.

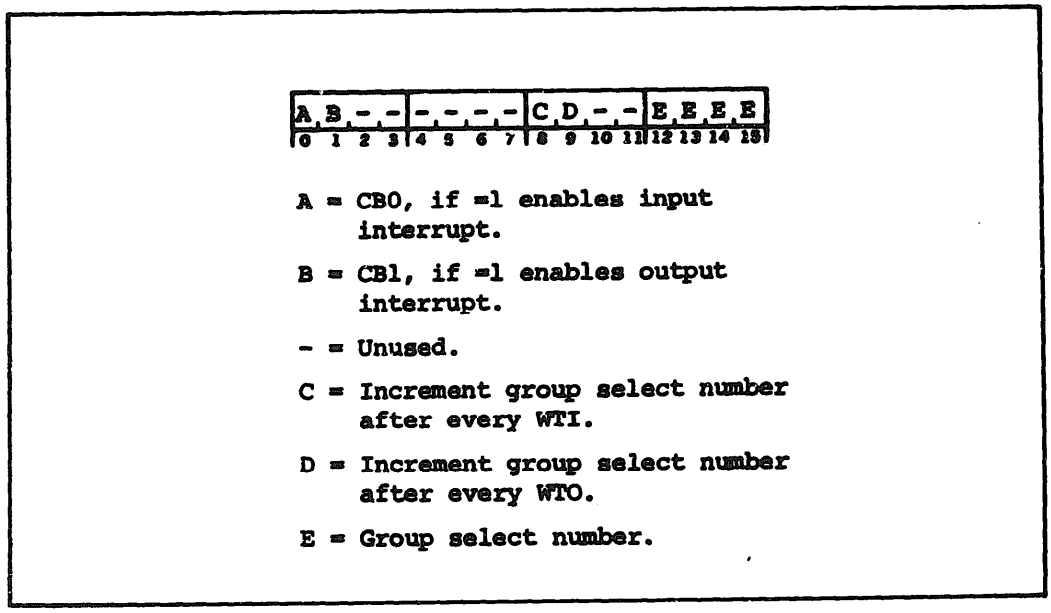


Figure 2-16. A-Register Format for EDF Command

The asynchronous I/O timing for the control of I/O data transfer is produced by a 4-MHz peripheral device clock signal (PCLK-). This clock signal establishes the timing relationship of the data being transferred between the processor and the using device

The system reset (SRST-) signal causes the controller to halt its current activity and return to an idle state. The controller is then ready to accept instructions, unless operator intervention is required. The SRST- signal is initiated either by a switch on the processor control panel or when primary power is applied or removed.

The strobe (STRB-) signal is produced and initiates the DDIOC I/O sequence. An I/O instruction word is used for control words. Control word content is used for data transfer as described in paragraph 2.3.2.2.

2.3.4 Theory of Operation

Detailed Input/Output data transfer sequence information is provided in GTE/IS manual H0011.

SECTION 3
OPERATING PROCEDURES

3.1 GENERAL

The DDIO Subsystem is used with and controlled by the CPU and the processor control panel. A brief summary of processor control panel operating procedures is provided in this section for reference purposes.

3.2 PROCESSOR CONTROL PANEL

Processor control panel operation is summarized in the following paragraphs. Complete operating procedures are provided in GTE/IS manual E0006.

3.2.1 Controls and Indicators

The processor control panel is shown in Figure 3-1. Processor control panel controls and indicators are described in Table 3-1.

3.2.2 Program Loading

The following describes program loading using the TTY paper tape reader. Loading from other devices is described in GTE/IS manual E0006.

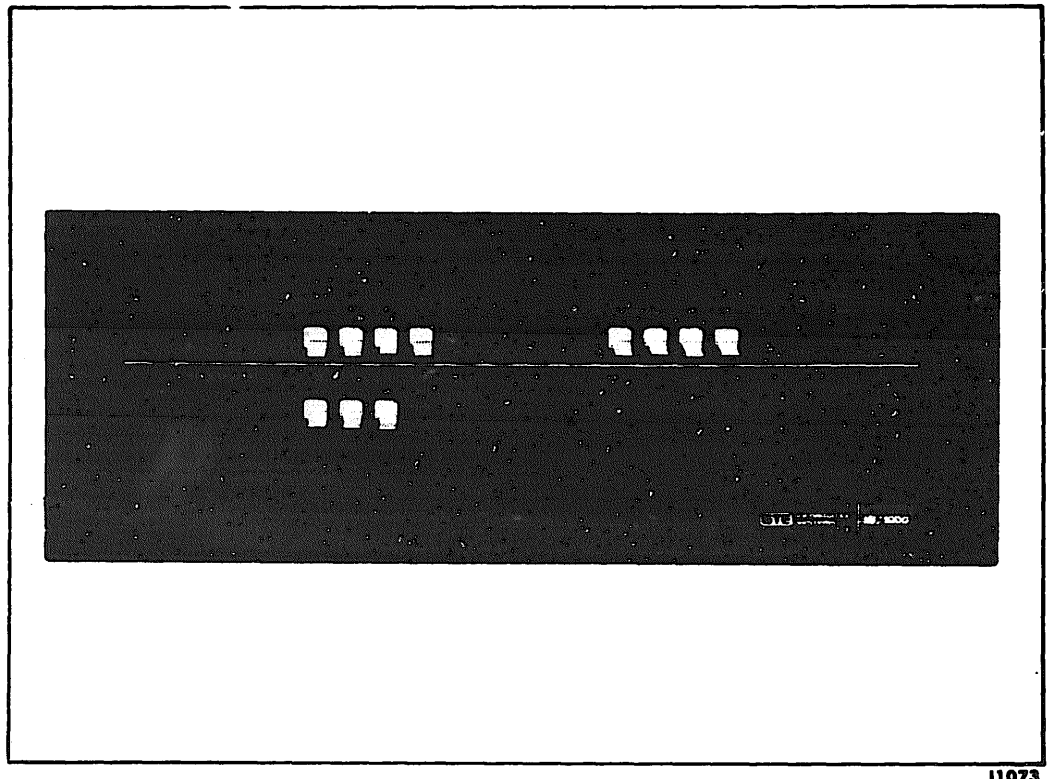


Figure 3-1. Processor Control Panel

Table 3-1. Processor Control Panel Functions (Sheet 1 of 5)

Switch or Indicator	Type	Function
LOCK/ON/OFF	Key Switch	Insertion of the key is required to turn this switch to any position. In the LOCK position, power is applied, but no switches are operative. The SENSE switches are considered to be in the down position when the key switch is in this position. In the ON position, power is applied and all panel switches and indicators are operative. In the OFF position, no power is available to the processor.
POWER	Indicator	Comes on when power is applied to the processor.
LOAD	Momentary	When raised and released, initiates automatic loading of a bootstrap program from the ROM into memory and puts the CPU in the run mode, executing the program loaded from the ROM. Actuating this switch with the power panel connected resets the system prior to automatic loading of the boostrap program.
RUN	Indicator	Comes on when the CPU is in the run mode.
LT	Indicator	Displays the contents of S-Register bit 8 ("less-than" condition).
GT	Indicator	Displays the contents of S-Register bit 9 ("greater-than" condition).
EQ	Indicator	Displays the contents of S-Register bit 10 ("equal-to" condition).
OVF	Indicator	Displays the contents of S-Register bit 11 ("overflow" condition).

Table 3-1. Processor Control Panel Functions (Sheet 2 of 5)

Switch or Indicator	Type	Function
0 thru 15 Data Entry	Toggle switches*	In the up position, these switches insert a ONE into the corresponding bit positions of the selected register when the MODE switch is in the WRITE position and the INITIATE switch is pressed.
0 thru 15 Data Display	Indicators	When the MODE switch is in the READ position, these indicators display the contents of the register SELECT switches. When the M Regi and I down), the INITIATE switch must be pressed before the contents of the memory location specified by the address in the P Register are displayed. When the MODE switch is in the WRITE position, these indicators display the contents of the data switches. An indicator that is lit (on) displays a ONE bit.
GP REGISTER/ SENSE 8, 4, 2, 1	Toggle switches*	ister. are down, the A Register (X-Register 0) is selected. When only the right-most swi B Reg four ary 1111). When the CPU is executing instructions, the switches act as program sense switches to allow external control over specified program operations. The up position specifies a logical ONE. The program can determine the stat instructions.

*Operative only when the LOCK/ON/OFF e CPU is in the halt mode

Table 3-1. Processor Control Panel Functions (Sheet 3 of 5)

Switch or Indicator	Type	Function
REGISTER SELECT P, I, M	Toggle switches*	The P and I switches, respectively, select the P or I Register when in the up position. In the up position, the M switch selects the M Register. When P, I and M are in the down position, the X Register specified by the GP REGISTER/SENSE switches is selected. When more than one switch is up, the leftmost switch has priority. Thus, to select the I Register, the P switch must be down. To use the M switch, the P and I switches must be down. The direction of transfer must be selected by setting the MODE READ/WRITE switch and, if an X Register is selected, the GP REGISTER/SENSE switches must be properly set.
MODE READ/WRITE	Toggle switch*	In the READ position, when the INITIATE switch is pressed and the M switch is selected (M switch up, P and I switches down), the contents of the memory location specified by the contents of the P Register are shown on the data display indicators. The contents of the P, I or a general-purpose register may be displayed simply by selecting the appropriate register. The INITIATE switch need not be pressed. In the WRITE position, when the INITIATE switch is pressed, information from the data switches is transferred to either the register selected by the P, I or GP REGISTER switches, or, if the M switch is selected, the memory location specified by the contents of the P Register.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

Table 3-1. Processor Control Panel Functions (Sheet 4 of 5)

Switch or Indicator	Type	Function
INITIATE	Momentary switch*	When the MODE switch is set to the WRITE position the INITIATE switch is pressed to enter information from the data switches into the selected register or memory. • The P Register when the P switch is up. • The memory location specified by the contents of the P Register when the M switch is up and the P and I switches are down. • The general-purpose register selected by the GP REGISTER switches when the P, I and M switches are down. NOTE: Data is not written into *the I Register.* When the MODE switch is set to the READ position, the M switch is selected and the INITIATE switch is pressed, the contents of the memory location specified by the contents of the P Register are shown on the data display indicators. When the MODE switch is set to the READ position, the contents of the following is displayed on the data display indicators: • The P Register when the P switch is up. • The I Register when the I switch is up and P is down. • The general-purpose register selected by the GP REGISTER switches when the P, I and M switches are down.
HALT	Momentary switch	When the CPU is in the run mode, pressing the HALT switch stops *program* execution at the completion of the instruction in process.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode

Table 3-1. Processor Control Panel Functions (Sheet 5 of 5)

Switch or Indicator	Type	Function
		When the CPU is in the halt mode: • If the M switch is selected, pressing the HALT switch increments the P Register and initiates a read/restore memory cycle. This has the effect of stepping through the memory and displaying the contents of each successive location on the data display indicators. Stepping through memory in this way displays the contents of successive locations but does not enable writing of data into memory, even if the MODE switch is set to WRITE. • If the M switch is not selected, pressing the HALT switch causes one instruction to be executed. This instruction is in the memory location specified by the contents of the P Register. After execution of the instruction, the P Register specifies the location of the next instruction to be executed.
RESET	Momentary switch*	Pressing this switch when the CPU is in the halt mode effects the CPU logic as follows: • Resets the arithmetic overflow flip-flop. • Resets the memory control flip-flops. • Resets the automatic program-load flip-flop and indicator. • Sets all N-Register flip-flops (unmasks all interrupts). • Resets all interrupt flip-flops. • Resets the interrupt control sequencer. • Readies the instruction-trap interrupt for service. • Readies the power-fail/restart interrupt for service. • Resets all device controllers on the I/O bus.
RUN	Momentary switch*	When pressed, starts automatic program execution with the instruction at the memory location specified by the contents of the P Register.

*Operative only when the LOCK/ON/OFF switch is in the ON position and the CPU is in the halt mode.

Perform program loading as follows:

1. Determine the type of ROM in the system: single-segment, four-segment, or two-segment. The TTY program is resident in the following ROM segments:
   - Single-segment ROM: segment I.
   - Four-segment ROM: segment I.
   - Two-segment ROM: segment II.
2. Perform program loading procedures for a specific ROM as follows:
   - Single-segment ROM - perform step 3.
   - Four-segment ROM - perform step 4.
   - Two-segment ROM - perform step 5.
3. Perform automatic loading of an absolute program using a single-segment ROM as follows:
   a. At the processor control panel, set the LOCK/ON/OFF switch to the ON position.
   b. At the TTY, place the punched tape copy of the appropriate absolute program in the TTY paper tape reader with any portion of the blank leader over the read station.
   c. Apply power to the reader mechanism by setting the LINE/OFF/LOCAL switch to LINE.
   d. d. Set the START/STOP/FREE switch to START.
   e. At the processor control panel, press the HALT switch.
   f. Press the RESET switch.
   g. Set the SENSE switches as shown in Table 3-2, to enable the desired function.
   h. Set the P, I, and M switches down.
   i. Lift and release the LOAD switch. A carriage return (CR) and line feed followed by a question mark are printed out on the TTY.
   j. At the TTY keyboard, type a period (.) to specify loading from the TTY paper tape reader.

      The punched tape is read by the TTY paper tape reader. When the checksum of the end-of-tape record is read, tape motion stops and the processor either halts or begins execution from the transfer address, depending on the setting of SENSE switch 2.

      The program loads into the processor core memory.
   k. If the operator desires to verify a tape after loading, proceed to step 1.
   l. Load the tape as described previously with SENSE switch 2 up.

Table 3-2. SENSE Switch Settings, Single-Segment ROM

Activity	SENSE Switch Settings (1)			
	8	4	2	1
Branch to transfer address after load.	-	-	D	D
Read tape and verify previous load.	-	-	D	U
Halt after load.	-	-	U	D
(1) D=down, U=up				

m. Rewind the tape and load it a second time with SENSE switch 1 up.

If an error is detected during either load operation, the processor halts with the I Register set to one of the values listed in Table 3-3. If loading is successful, the I-Register value is $1.

4. Perform automatic loading of an absolute program using four-segment ROM as follows:

a. Ready the program on the input device (steps 3a thru 3d).

b. At the processor control panel, press HALT then RESET.

c. Set the SENSE switches as follows:

- 8 down.
- 4 down.
- 2 up if it is desired to halt the program just loaded before control is transferred to it.
- 1 up if it is desired to halt the program to inspect and/or enter configuration data into the processor A and B Registers.

d. Set P, I, and M down.

e. Lift and release LOAD. If SENSE switch 1 is down, the program loads into the processor core memory.

A halt occurs with any of the I-Register values shown in Table 3-4.

Table 3-3. Tape Load Halts, Single-Segment ROM

I-Register Value	Meaning
$1	Successful load.
$F	Checksum error.
$1F	Verify error.
$2F	I/O instruction rejected.
$3F	Load error.

Table 3-4. Tape Load Halts, Four-Segment ROM

I-Register Value	Meaning	Recovery
2	Enter configuration data in A Register.	Enter data and press RUN.
$3B	Halt prior to branching to program.	Press RUN.
$F	Bad checksum on last record.	Restart ROM.
$F	Check checksum on record last read.	Restart ROM by pressing RUN.
$0	I/O instruction reject.	Restart ROM at P=$55.

f. Enter or inspect configuration data in the A and B

- A Register:

Bits	Use
0 thru 3	Unused.
4 thru 7	Interrupt line.
8 thru 9	Unused.
10 thru 15	Device address.

- B Register - Not used.

g. **Press RUN.** The program loads into the processor core memory.

5. **Perform automatic loading of an absolute program using two-segment ROM as follows:**

a. **Ready the program** on the input device (steps 3a thru 3d).

b. Press HALT and then RESET.

c. Set the SENSE switches as follows:

- 8 up.
- 4 up.
- 2 up if it is desired to halt the program just loaded before control is transferred to it.
- 1 down.

d. Set P, I, and M down.

e. Lift and release LOAD. The program loads into the processor core memory.

SECTION 4
INSTALLATION

4.1 GENERAL

This section provides the basic installation procedures and associated information for the DDIO Subsystem.

4.2 SITE REQUIREMENTS

Site requirements applicable to the DDIO Subsystem are listed in the following paragraphs.

4.2.1 Environmental Requirements

Temperature and humidity limitations for the DDIO Subsystem are as follows:

Environmental Characteristic	Storage	Operation
Temperature:	-32°C to +57°C	+20° to +35°C
Humidity:	5 to 90% relative without condensation	30 to 90% relative without condensation

4.2.2 Power Requirements

Power to the DDIOC is provided by the IS/1000 power supply through connector P14. The IS/1000 power supply rectifier assembly requires input power of 115 ± 10 Vac, 55 ± 8 Hz at 6.6 A maximum.

Power to the DDIOB is provided by the Communications Power Supply. The Communications Power Supply requires input power of 115 ± 10 Vac, 55 ± 8 Hz, at 4.5 A maximum.

4.3 UNPACKING AND PACKING

Carefully remove packing materials, braces, and/or fastening materials. Store reusable materials with shipping containers.

When shipping equipment, ensure that insulation and container are fully protective.

4.4 CABLING

DDIO Subsystem cabling is shown in Figure 4-1. Pin assignments for PC board connectors are provided in Appendix B. Cable assembly wire lists appear in Appendix C.

4.4.1 I/O Bus

I/O bus cabling from the processor to the DDIOC is accomplished by 50-conductor ribbon cables with PC connectors. The I/O bus is distributed on two cables from the processor to connectors J1 and J2 on the controller assembly.

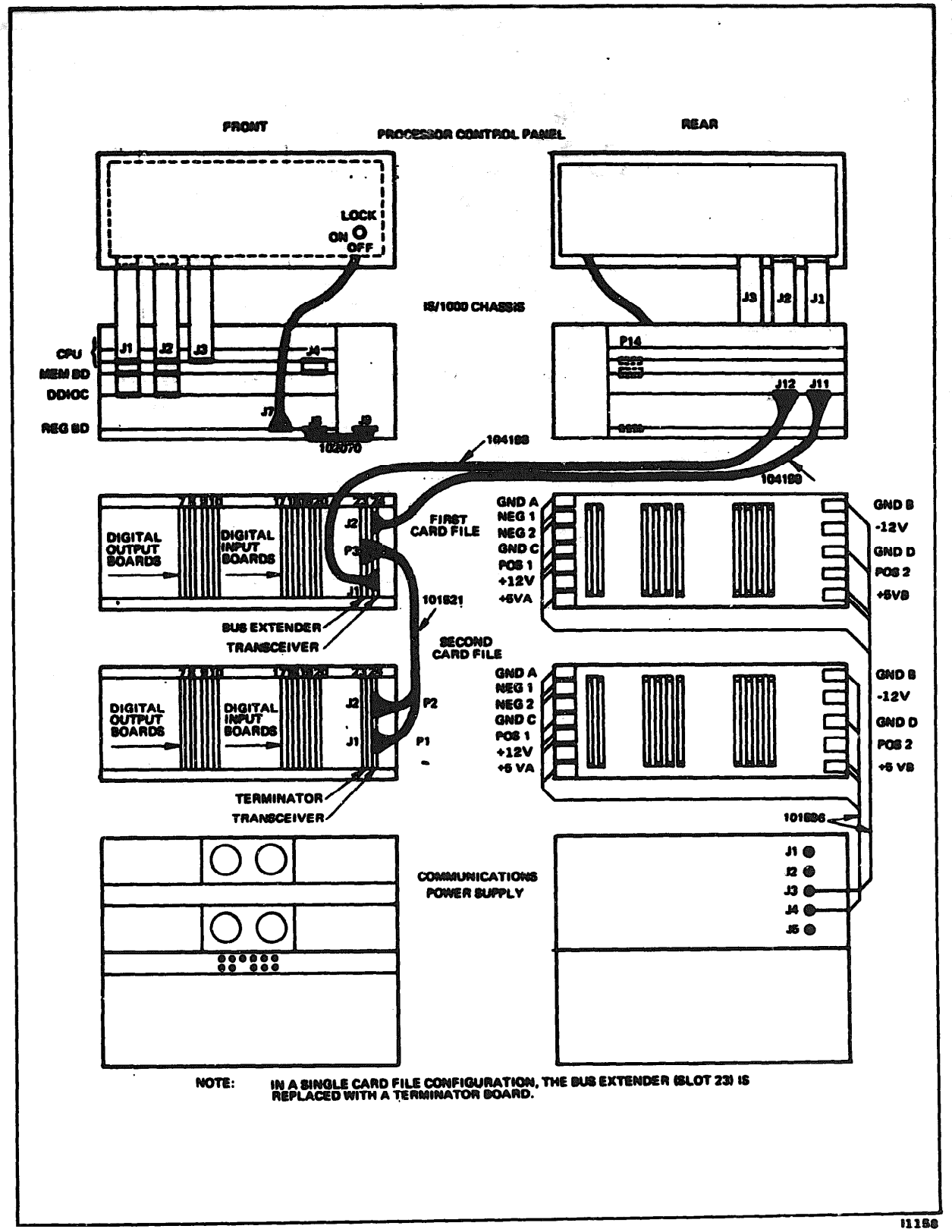


Figure 4-1. DDIO Subsystem Cabling

4.4.2 DDIOC/Card File

Edge connector J11 on the DDIOC attaches to connector J2 on the first card file transceiver board using the Data cable assembly (104199). DDIOC edge connector J12 attaches to connector J1 on the first card file transceiver board using the Control cable assembly (104198).

Edge connector P14 on the DDIOC plugs into the power backplane receptacle J14, coupling the DDIOC to the chassis power supply.

4.4.3 Communications Power Supply/Card File

Power cables 101596 utilize connectors J3 and J4 on the Communications Power Supply. Connector J3 attaches to the first card file and, if necessary, J4 attaches to the second card file. The card file ends of the cable are branched and terminated with press-on terminals. Each branch is identified with the mnemonic of the card file backplane terminal to which it connects, e.g., the branch tagged as GND A connects to terminal GNDA.

4.5 PATCHING

The DDIOC contains manually alterable patches for the CPU DDIO address, common interrupt response to the CPU, and DDIO identification response to the CPU. These patches are installed at the time of installation and reflect the system configuration. If system requirements change, the patch jumper wires are changed to conform to the new configuration. The patch connections are shown in the System Configuration Specification.

The location and function of the patches used are lised in Table 4-1. Specific requirements for each of the three patch functions are as follows:

4.5.1 Device Address Patches

Patches in board locations 4A and 4C form the A address decode. Patches in board locations 4D and 4B form the B address decode.

4.5.2 Input Interrupt Patches

A direct interrupt line assignment, or common interrupt line assignment is selected by a jumper on the patch in location 7A. The jumper may be changed to conform to the system configuration.

4.5.3 ICI Response Patches

When a common interrupt line is used, a jumper in the patch at either location 7B or 7C is installed. The controller designation may be changed to conform to the system configuration.

Table 4-1. DDIOC Patch Locations and Functions

Function	Location
Device address A, DA00 thru DA02	4C
Device address A, DA03 thru DA05	4A
Device address B, DA00 thru DA02	4B
Device address B, DA03 thru DA05	4D
Input interrupt, level 8 thru 15	7A
ICI response, DIB00 thru DIB07	7B
ICI response, DIB08 thru DIB15	7C
	Refer to Appendix D-1, Sheet 2.

4.6 ADJUSTMENTS AFTER INSTALLATION

After installation of the DDIO assemblies, verify correct communications power supply voltages as described in GTE/IS manual B0037.

4.7 TESTS AFTER INSTALLATION

After installation or a prolonged idle period, execute the performance tests described in Section 6.

4.8 REMOVAL AND REPLACEMENT

The following paragraphs describe removal and replacement of the various DDIO Subsystem assemblies.

WARNING

- *Before performing any procedures described in this section, all power must be removed from the unit and chassis.*
- *When removing power cables, always remove connector from power source first.*

Failure to observe these warnings can result in injury to personnel and/or damage to equipment.

CAUTION

All units and cabling must be handled with care to prevent damage. Connector contacts must be kept clean and unobstructed.

4.8.1 Removal, DDIOC

To remove the DDIOC PC Board from the chassis:

1. **Set the processor control panel LOCK/ON/OFF switch to OFF.**

2. If the control panel obstructs access to the PCBA:

   a. Unscrew two large thumbscrews on far left- and right-hand sides of panel. Be sure to support the panel with one hand while loosening the screws since they are the only support for the panel.

   b. Carefully disconnect cables J1, J2, and J3 attaching the panel to the CPU.

   c. Disconnect cable from Regulator Board connector J7.

3. Remove the PCBA retaining bracket (left side).

4. Disconnect all cables from the front and rear of the board.

5. From the front of chassis, pull evenly on both sides of the board. After the board disengages from the backplane power connector (J14), it should slide out easily.

6. Place board on cushioning or in an appropriate container.

4.8.2 Installation, DDIOC

To install the DDIOC PC Board in the chassis:

1. Set the processor control panel LOCK/ON/OFF switch to OFF.

2. If the control panel obstructs access to the PCBA slot:

   a. Unscrew two large thumbscrews on far left- and right-hand sides of panel. Be sure to support the panel with one hand while loosening the screws since they are the only support for the panel.

   b. Carefully disconnect cables J1, J2, and J3 attaching the panel to the CPU.

   c. Disconnect cable from Regulator Board connector J7.

3. Clean all PCBA connectors with a cotton swab dipped in Freon TF or isopropyl alcohol.

4. Guide the rear (P14 connector end) of the board into the chassis slot making sure the board is properly engaged with the guides on both sides of the board.

5. Gently slide in the board until the power connector (P14) contacts the chassis backplane power connector (J14).

6. Press firmly on the front of the board until it rests completely in J14.

7. Install the PCBA retaining bracket (left side).

8. Connect all cables to PCBA.

9. If the control panel has been removed:

   a. Connect cable to Regulator Board connector J7.

   b. Carefully connect cables J1, J2, and J3 from the control panel to the CPU.

   c. Supporting the control panel with one hand, install and tighten two large thumbscrews on far left- and right-hand sides of panel.

4.8.3 Removal, Card File PCBA

To remove a PC board from a DDIO card file:

1. Turn power off.
2. Remove card file front cover.
3. Disconnect cable(s) from front of board.
4. Pull evenly on top and bottom of board. After board disengages from backplane connector, it should slide out easily.

4.8.4 Installation Card File PCBA

NOTE: Card file slot positions for DDIO Subsystem PC boards are provided in Figure 4-2.

To install a PC board in a Line Switch card file:

1. Turn power off.
2. Guide front of board into proper card file position. Check that board is properly engaged with guides on top and bottom.
3. Gently slide board in until it contacts backplane and card file. Sliding should be smooth and easy. If obstruction is encountered, do not force board. Remove and investigate problem.

   When board contacts backplane, press firmly on board until it seats completely in backplane connector.
4. Connect cable(s) to front of board.
5. Install card file front cover.

4.8.5 Removal, Card File

To remove a DDIO card file:

1. Turn power off.
2. Remove all boards from card file (paragraph 4.8.4)
3. Swing Communications Power Supply out to servicing position.
4. Disconnect power connections from rear of card file backplane.
5. At front of cabinet, remove four screws from card file.
6. Carefully lift card file out of cabinet.

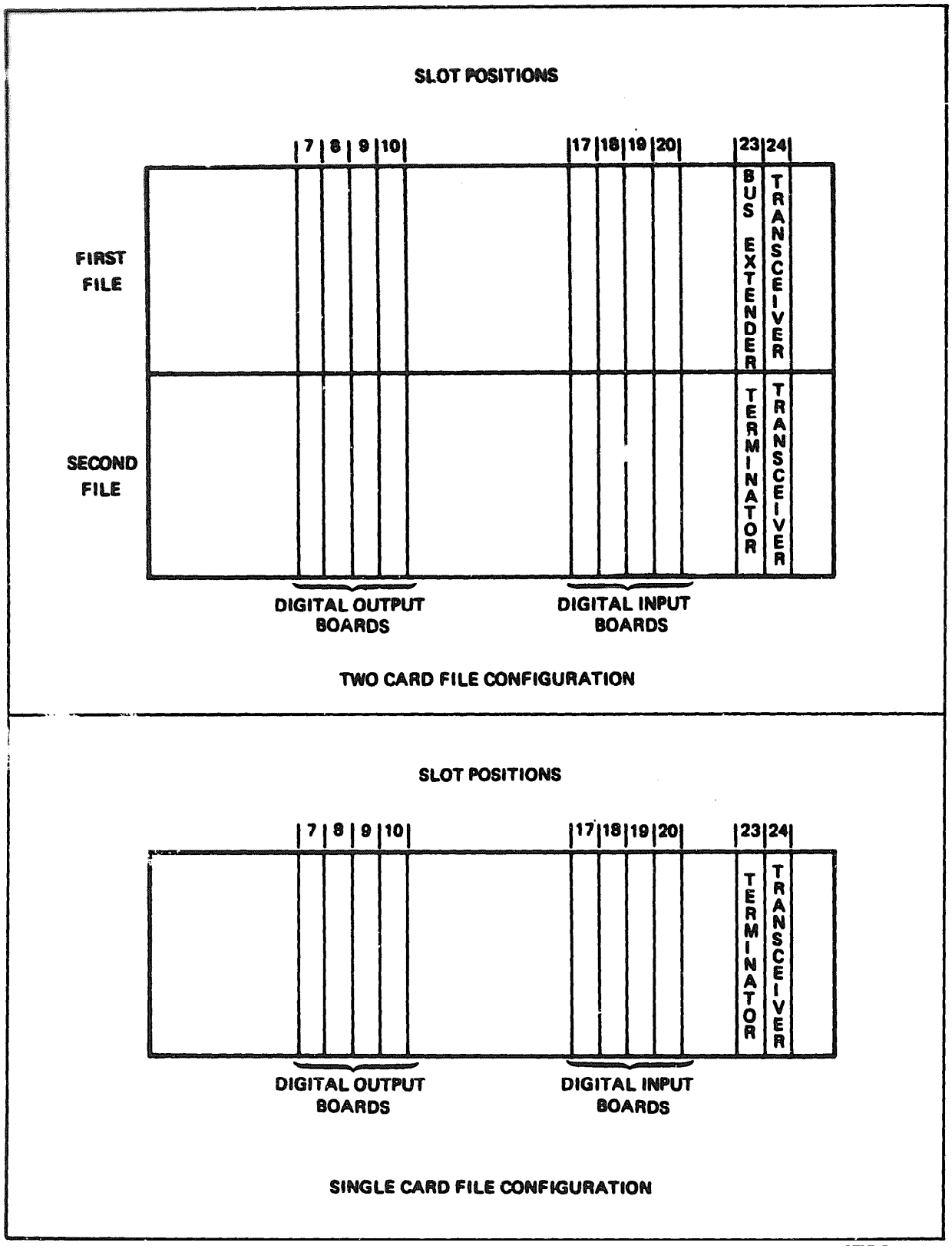


Figure 4-2. Card File PC Board Slot Positions

4.8.6 Installation, Card File

To install a Line Switch card file:

1. **Turn power off.**
2. **At front of cabinet, carefully position card file between vertical mounting rails at desired location. Mounting flanges of card file must be on outside of vertical mounting rails.**
3. **Secure card file with four screws through mounting flanges.**
4. **At rear of cabinet, swing Communications Power Supply out to servicing position.**
5. **Connect all power supply connections to rear of card file backplane** (Figure 4-1).
6. **Install required boards in card file** (paragraph 4.8.4).

4.8.7 Removal, Communications Power Supply

To remove a Communications Power Supply:

1. **Set PWR switch on communications power supply to off (down) position.**
2. **Remove two #10 screws on right-hand flange of power supply and swing out to servicing position.**
3. **Disconnect all cables from rear of power supply.**
4. **Carefully lift power supply off hinges.**

4.8.8 Installations, Communications Power Supply

To install a Communications Power Supply:

1. **Set PWR switch on communications power supply to off (down) position.**
2. **Carefully install power supply on hinges in cabinet.**
3. **Connect all cables to rear of the power supply.**
4. **Secure right-hand flange of power supply to cabinet with two #10 screws.**

4.8.9 Removal, Communications Power Supply PC Boards

To remove the Communications Power Supply PC Boards:

1. **Set PWR switch on communications power supply to off (down) position.**
2. **From front of power supply, remove retaining bar, secured by two fasteners.**
3. **Pull evenly on both top and bottom of board. After board disengages from motherboard, it should slide out easily.**

4.8.10 Installation, Communications Power Supply PC Boards

To install Communications Power Supply PC Boards:

1. **Set PWR switch on communications power supply to off (down) position.**
2. **Guide front of the board into proper chassis position. Ensure that board is properly engaged with guides on top and bottom.**
3. **Carefully slide board in until it contacts motherboard. Sliding should be smooth and easy. If an obstruction is encountered, remove board and investigate problem.**
4. **Press firmly on PC board until it seats completely in motherboard assembly.**
5. **Install board retaining bar and secure with two fasteners.**

SECTION 5
MAINTENANCE

5.1 GENERAL

This section contains preventive and corrective maintenance information. Corrective maintenance information in this section is limited to isolating and correcting assembly-level malfunctions.

5.1.1 Maintenance Procedure

Figure 5-1 is a maintenance guide for the DDIO Subsystem. The procedural flow is such that only correctly operating equipment will allow the service representative to "end" maintenance.

The reference column of Figure 5-1 directs the user to supporting sections and paragraphs of this manual, unless otherwise noted. When a reference is made to "manuals supplied with the equipment", the other manuals supplied depnd on the system configuration. All applicable manuals are listed on Document Configuration Records sent with the support documentation.

5.1.2 Service Logs and Reports

Maintenance of a service log is recommended in which to record daily, the length of service of the equipment, and, if convenient, the type of programs being run. This log can be used to help determine preventive maintenance periods and to register the length of service between failures. Recording the type of application program being run (if more than one is used) may show a trend of equipment failures during certain types of programs.

Service reports to establish a case history for each unit should be kept by the user. These records should include particulars of all work done on the equipment and should be kept up-to-date as a useful reference for the service representative.

5.2 PREVENTIVE MAINTENANCE

Preventive maintenance includes periodic inspection, cleaning, and testing to verify proper operation. Associated with these tasks are the maintenance of service logs and reports that can be used to indicate performance trends.

5.2.1 Periodic Maintenance

Table 5-1 contains a preventive maintenance checklist with procedures to be performed at specified intervals to help ensure that satisfactory operating conditions are maintained.

5.2.2 Measuring Power Supply Voltages

Power supply voltages for the DDIOC can be measured at the backplane power connector, J14, through access holes in the back panel of the chassis. Table 5-2 lists the normal voltage for each test point.

Communications power supply voltages are measured at the test points provided on the front of the power supply chassis. The normal voltage present at each test point is listed in Table 5-3.

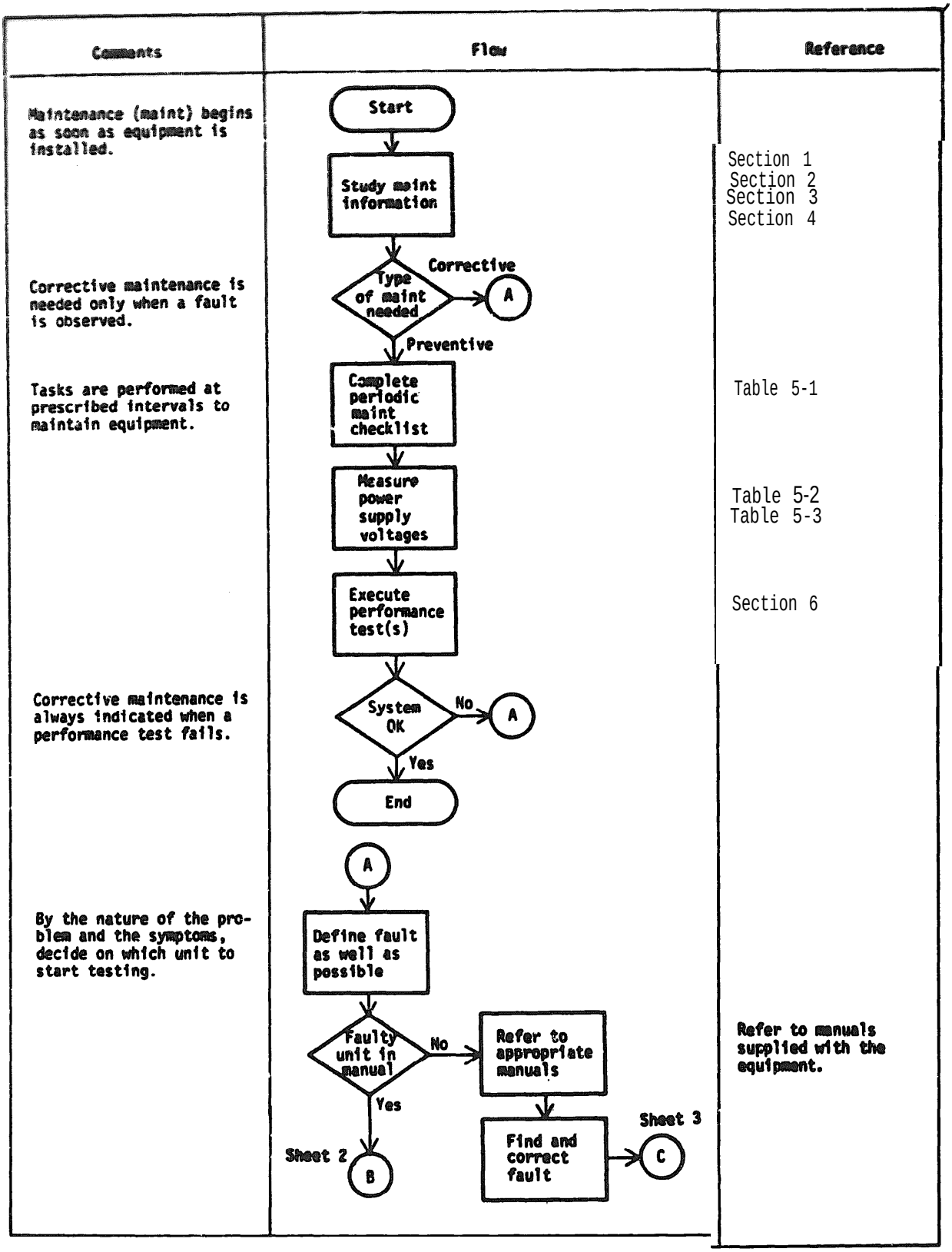


Figure 5-1. DDIO Subsytem Maintenance Guide (Sheet 1 of 4)

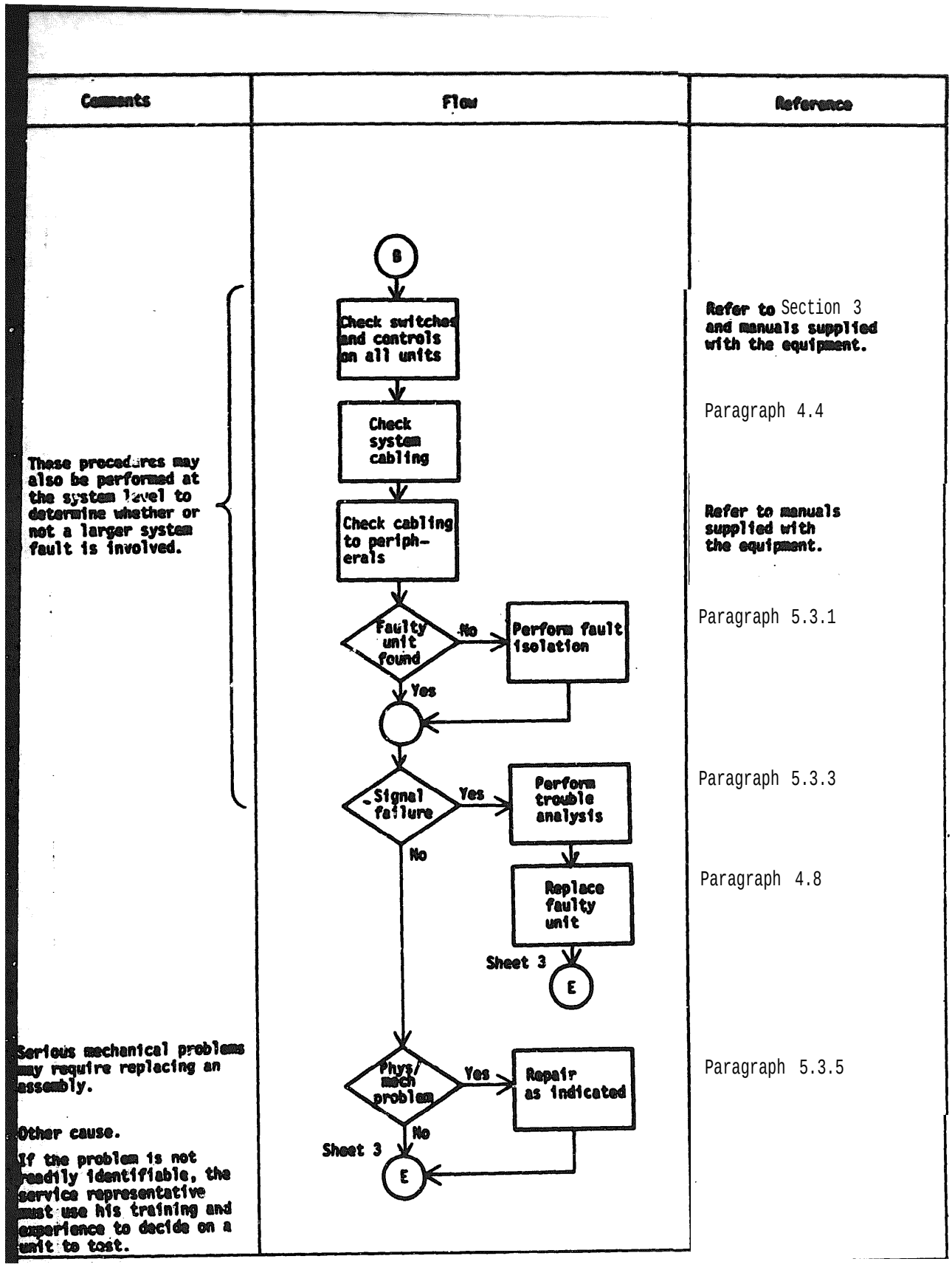


Figure 5-1. DDIO Guide (Sheet 2 of 4)

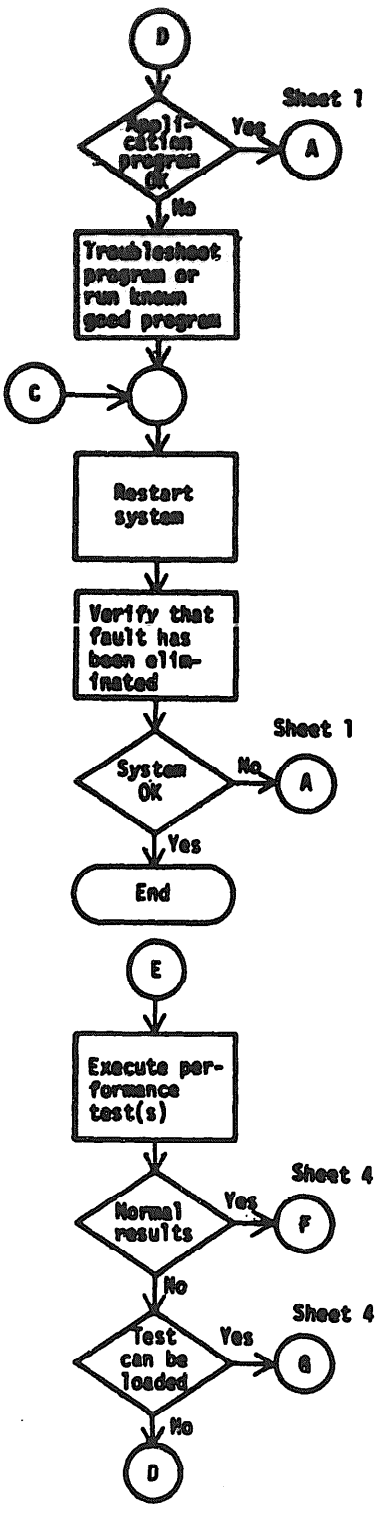
Comments	Flow	Reference
Sometimes an unproven program or subroutine appears to be a system failure. The help of a programmer may be needed.		Paragraph 5.3.4
This is an important last step in any maintenance procedure. Performance tests are the heart of the corrective maintenance procedure. Loads and executes with normal errors. Inconclusive result. Loads and executes with no errors. Wrong unit may have been tested or the application program demonstrating the original failure may be suspect.		Section 6

Figure 5-1. DDIO Subsystem Maintenance Guide (Sheet 3 of 4)

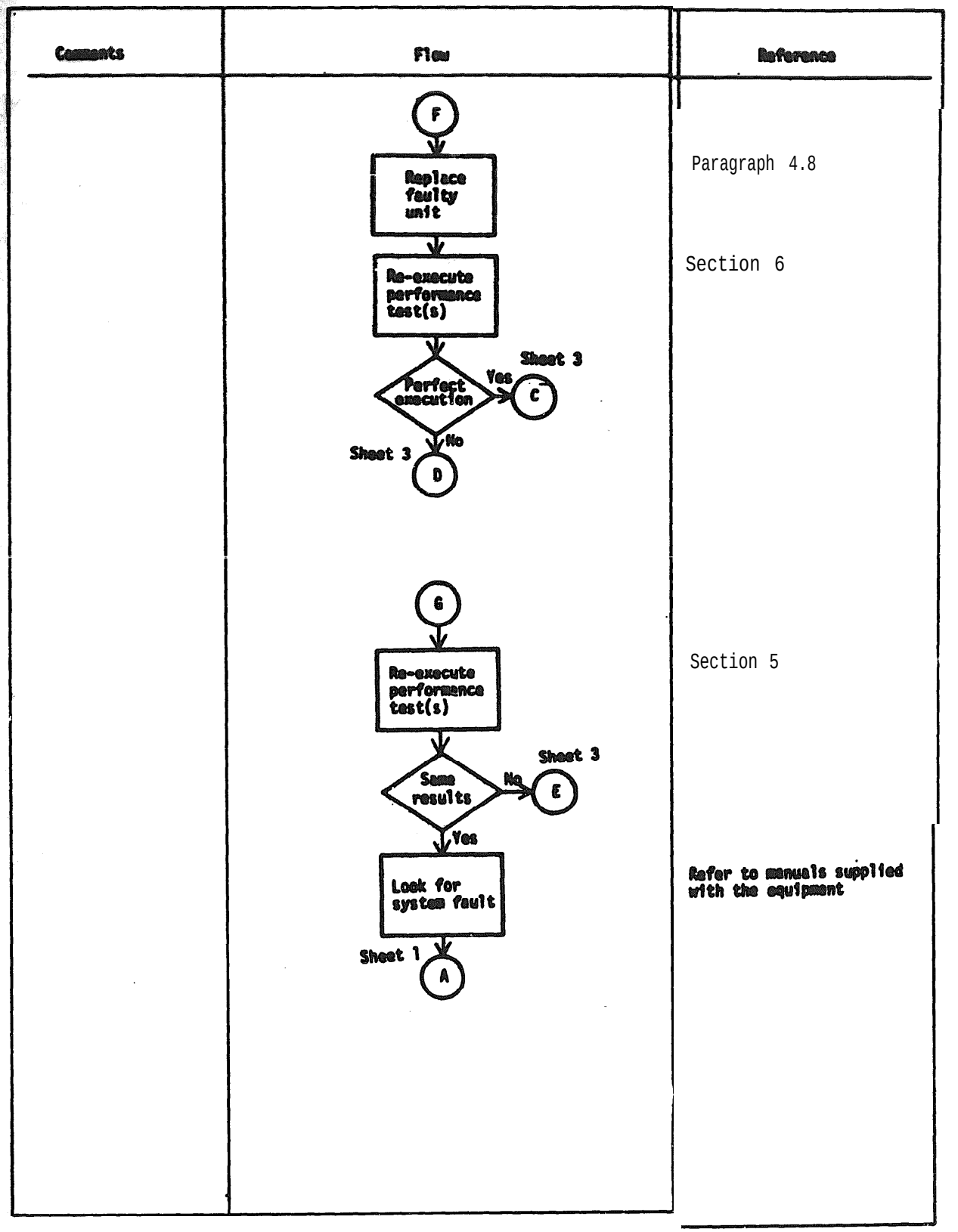


Figure 5-1. DDIO subsystem Maintenance Guide (Sheet 4 of 4)

Table 5-1. Preventive Maintenance Checklists

Task	Interval	Procedure
Execute performance test.	As required.	Execute the appropriate performance test, given in Section 6, after maintenance has been performed or after the unit has been idle for an extended period.
Inspect cables.	4 months.	Look for frayed cables and wires. Check to be sure that no wires are squeezed between structural members. Inspect conenctors for damage.
Measure power supply voltages.	12 months or during trouble-shooting periods.	Refer to paragraph 5.2.2.
Inspect connector pins.	12 months.	Verify that there are no bent or spread connector pins, particularly on plug-in IC connectors. Careless installation often causes spreading of pins.
Clean connectors.	12 months.	Dissolve and wipe away grease deposits with a cotton swab dipped in Freon TF* or alcohol. All connectors are gold plated and must not be burnished.
Inspect resistors	12 months.	Verify that discoloration of coding bands or loss of coating (indicating abnormal power dissipation) has not occurred.

*Do not use Freon on 3M connectors

Table 5-2. Power Backplane Test Points

Test Point	Output
GND	Ground
+5V	+5.0 ± 0.5 Vdc
PFR (power failure reset)	+5 Vdc (normal)
60HZ (clock signal)	60 Hz at +15 ± 2 Vac
RESET (master)	+5 Vdc (normal)
-12V	-12.0 ± 0.6 Vdc
+12V	+12.0 ± 0.6 Vdc

Table 5-3. Communications Power Supply Voltage Measurement Points

Test Point	Source of Signal (board)	Voltage or Signal
TP1	+10-Vdc rectifier and +5-Vdc regulator	+5.00 ± 0.05 Vdc
TP2	+5-Vdc regulator (1)	+5.00 ± 0.05 Vdc
TP3	+5-Vdc regulator (2)	+5.00 ± 0.05 Vdc
TP4	+12-Vdc rectifier and regulator	+12.00 ± 0.12 Vdc
TP5	-12-Vdc rectifier and regulator	-12.00 ± 0.12 Vdc
COM (TP6)	Motherboard	Common reference

5.3 CORRECTIVE MAINTENANCE

Information in the following paragraphs is provided to aid in isolating DDIO Subsystem malfunctions and correcting those malfunctions to the assembly level.

5.3.1 Fault Isolation

The following preliminary tests and checks should be performed to help eliminate simple problems:

- Check switches and controls on all units to be sure that settings are correct for the application that is failing. Occasionally something as simple as a required switch setting is overlooked when running the system.
- Check I/O and power connectors to be sure that all connectors are firmly seated at the proper receptacles.
- Verify that all units are connected to a correct source of power.

The heart of fault isolation is the performance tests. A comprehensive set of performance tests have been developed for the DDIO Subsystem. Descriptions of these test programs and instructions for their use are provided in Section 6.

Occasionally, a general failure of the equipment is encountered, involving the power supplies or a basic timing signal. Power supply maintenance and general signal tracing procedures are provided in GTE/IS manuals A0003 and B0037.

Logic diagrams for the DDIO Subsystem are provided in Appendix D.

5.3.2 Servicing

5.3.2.1 DDIOC

To install the DDIOC in the test slot, perform the following:

1. Remove DDIOC by performing the procedures of paragraph 4.8.1
2. Slide chassis from cabinet.
3. Remove chassis top cover.
4. Install DDIOC in test slot by performing the procedures of paragraph 4.8.2.
5. Set processor control panel LOCK/ON/OFF switch to ON.
6. When servicing has been completed, install DDIOC in operating position by reversing the preceding procedures

5.3.2.2 Communications Power Supply

Servicing information for the Communications Power Supply is provided in GTE/IS manual B0037.

5.3.3 Trouble Analysis

Analysis of trouble discovered during fault isolation is considered for three types of failures:

- Test program failures.
- Signal failures.
- Physical/mechanical.

5.3.3.1 Test Program Failure

Test programs can produce one of three results, as described in the following paragraphs.

If a test program loads and executes with no error indications, the wrong board may have been tested or the fault may be in the user application program. Unless a user program has previously operated successfully, the program should be considered the probable cause of the failure. Refer to paragraph 5.3.4 or program troubleshooting suggestions.

If a test program loads and executes with normal error indications, the fault is probably within the board being tested.

If a test program cannot be loaded properly, or if execution of a program leads to gross error indications or erratic performance, the test must be considered inconclusive. Try again to load and execute the test program. If the same results are obtained, a larger system malfunction may be indicated.

Continue with trouble analysis steps to establish whether the DDIO Subsystem is actually at fault.

5.3.3.2 Signal Failures

Incorrect signals from peripheral equipment must be diagnosed and corrected using manuals supplied with the equipment.

5.3.3.3 Physical/Mechanical Failures

Broken wires, damaged components, loose connectors, etc. are self indicative of the required solution. Cable wire lists are provided in Appendix C.

To to determine what caused the trouble or, at least, try to rule out the trouble as a symptom of a more serious problem.

5.3.4 Programs Troubleshooting

When a problem occurs while running an application program and the suspected equipment successfully executes the test programs provided, the application program must be considered the probable cause of the failure.

One method of debugging a program is the progressive insertion of branch instructions around each major section of the program.

NOTE: ***When troubleshooting in this manner, be careful not to branch around essential controller initialization instructions.***

Once the general area of the fault is determined, the specific instruction(s) causing the failure must be found. Detailed knowledge of the specific program is needed to continue an analysis.

The task of finally producing a working program may become the responsibility of a programmer; however, the service representative should verify whether the program has thus been eliminated as the cause of the failure.

5.3.5 Repair

Repair of the DDIO Subsystem below the assembly level is beyond the scope of this manual. When component-level troubleshooting and replacement are required, the service representative must rely on his training and experience, his skill with test equipment and his ability to use the system support maintenance documentation.

5.3.6 Verifying Proper Operation

An important last step in any maintenance procedure is to follow repairs with a performance test. This ensures that all faults have been isolated and corrected by verifying proper equipment operation. Refer to Section 6.

SECTION 6
PERFORMANCE TESTS

6.1 GENERAL

This section describes the DDIO performance test program (TESDDIO). Test operating procedures and an explanation of error indications are also included.

A performance test should be run after:

- The subsystem units are installed.
- An extended idle period.
- Corrective maintenance has been performed.

6.2 DESCRIPTION

The TESDDIO program provides a check of the performance of DDIO components and its interfaces. The test program is comprised of a series of test subprograms designed to exercise specific DDIO component functions. Error codes enable isolation of faults.

TESDDIO is executed by the processor under control of the Test Executive Program (T2SEXC).

Brief descriptions of the TESDDIO test routines are provided in the following paragraphs.

6.2.1 Command Acceptance Test (CA)

The CA test subprogram executes all I/O instructions that the DDIO recognizes. It checks the proper operation of the command, address, and EKO circuits. The program detects an error if the DDIO does not respond with an EKO signal for a legal instruction. The command error is printed. Each accepted address causes a program halt. Operator verification is required.

6.2.2 Group Selection Test (GS)

The GS test checks the DDIO group selection circuits. All groups are selected by a programmed EDF Command word instruction.

After a group has been selected, a programmed RDS instruction obtains the device status to verify correct group selection. All 16 groups are checked incrementally in this manner. Errors may be printed on the TTY.

6.2.3 Increment Group Test (IG)

The IG test checks the incrementing circuits of the group select counter after each WTO and WTI instruction.

Group 0 is automatically selected. A programmed WTO instruction is produced to advance the select counter. An RDS instruction follows to check the counter status. The two instructions are repeated until group 15 is reached. The same process is used with the WTI instruction. Errors may be printed on the TTY.

6.2.4 Move Bit Test (MB)

The MB test selects an input and output group and transmits bit 15. It then checks that the bit is returned. This process is repeated for all bits of the group. The bits are left shifted into and stored in the processor A-Register. Errors may be printed on the TTY.

6.2.5 Incrementing Pattern Test (IP)

The IP test selects an input and output group, and then sequences a bit through the loop. The bit position is compared with a bit in the A Register. Any mismatch may cause an error to be printed on the TTY. The count is incremented by one bit until count $FFFF is reached.

6.2.6 Basic Test (BT)

The BT test program enables sequential processing of all test programs. The CA test is performed checking only the configured address. Errors may be printed on the TTY.

6.2.7 Intermediate Test (IR)

The IR test checks the intermediate register (output data buffers) in the controller. An EDF CWD selects a group. A WTO with a value of $0000 is then produced. A WTI-7 is produced to allow comparison of the contents of the data buffers and A-Register. Data is shifted left and stored in the A-Register. Errors may be printed on the TTY.

6.2.8 Select Test Module Test (SM)

By entering SM, the operator may select the sequence in which the test programs are executed. In addition, the passes of the test program may be specified.

Up to thirteen test programs may be executed in one pass.

6.2.9 Error Queue (EQ)

Accumulated errors up to a maximum of ten, together with the total error count, are printed on the TTY after the operator types EQ (CR) in response to RUN. The errors are accumulated since the last EQ test.

The error queue table is cleared after each routine. The maximum number of errors accumulated is $FFFF. The error count goes to $0000 on the detection of the next error.

6.3 PREREQUISITES

The following equipment, or equivalent, is required to perform TESDDIO:

- GTE/IS Model IS/1000 Communications Processor (with 8K memory) which includes a GTE/IS Model 4821-01 Processor Control Panel (102291).
- Teletype Corporation Model ASR/KSR-33 or ASR/KSR-35 Teletypewriter Set (TTY), modified to include a TTY interface (100505).
- GTE/IS Model 5210-01 Utility Controller and Distributor.
- DDIO Test Cable Assembly (104208) for MB, IP, BT, and SM tests.

A Tektronics Model 7403N oscilloscope, or equivalent, is recommended test equipment for troubleshooting.

An extender assembly, 101158 or equivalent, is recommended for troubleshooting card file PC board errors.

The TESDDIO and T2SEXC tape is required to perform TESDDIO.

6.4 TEST SETUP

The normal test setup for performing the TESDDIO test program is shown in Figure 6-1.

6.5 OPERATING PROCEDURES

General procedures for performing TESDDIO are provided in the following paragraphs. Test operation options are provided in paragraph 6.6.

1. At the processor control panel, set the LOCK/ON/OFF switch to ON.
2. At the TTY, set the LINE/OFF/LOCAL switch to LINE.
3. At the processor control panel, set all the SENSE switches to the down position (off).

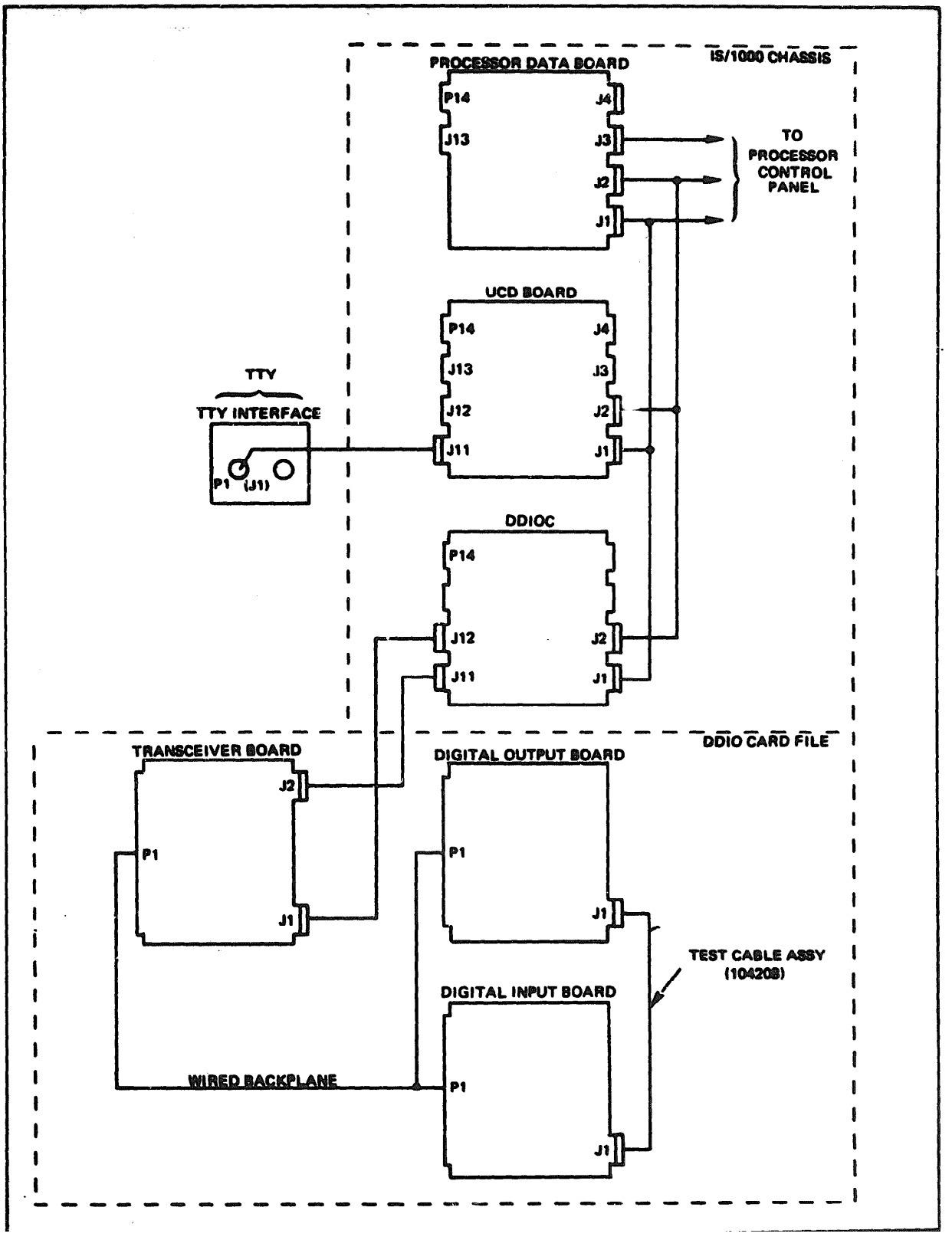


Figure 6-1. TESDIO Test Setup

4. When T2SEXC and TESDDIO are loaded, via the available media, enter the desired control parameters via the TTY keyboard, followed by a CR. The input format and meaning of each control parameter are listed in Table 6-1.

NOTE: If an error is made in an operator input, an up-arrow (↑) may be typed at the TTY, followed by the correct entry.

When the last control parameter has been entered, the TTY prints out:

RUN

At this point, TESDDIO has been configured and T2SEXC is ready to accept a selected test.

5. At the processor control panel, set the SENSE switches as shown in Table 6-1. to enable the function desired.

At the TTY, type the two-character test identifier (Table 6-3) for the test routine to be run, followed by a comma, in response to RUN.

7. Type a decimal number from 1 thru 32767 (pass count) followed by a CR. This entry specifies the total number of test cycles to be performed and initiates execution of the test specified.

Permissible responses to the RUN statement are as follows:

- RUN ID, PASS COUNT
- RUN ID CR.
- RUN CR.

If the pass count is omitted (RUN ID CR), the test is repeated until halted by the operator or an error is detected.

If the RUN CR response is used, the program executes the test previously specified.

8. During execution of some test routines, the program may require action by the operator or provide information pertinent to the test. Table 6-4 lists the headings that may be output and indicates the proper action required or gives their meanings.

On completion of the test, the TTY prints out:

COMPLETION

Table 6-1. TESDDIO Control Parameters (Sheet 1 of 2)

Control Parameter Request	Operator Input
DDIO OUTPUT DEV. ADDR=	*NOTE: The device address is entered in hexadecimal values, all others are entered in decimal. Either number system can be used if the conversion to an equivalent system is made.* *All control parameter inputs must be followed by a CR.* Decimal (0 thru 63) or hexadecimal ($0 thru $3F) number of DDIO output device address.
DDIO INPUT DEV. ADDR=	Decimal (0 thru 63) or hexadecimal ($0 thru $3F) number of DDIO input device address.
OUTPUT INTERRUPT ENABLED (Y OR N)=	Y for a direct interrupt. Or N for an I/O interrupt.
DDIO OUTPUT INT LINE=	Decimal (8 thru 15) or hexadecimal ($8 thru $F) number of DDIO interrupt level (A-bus interrupt to processor).
DDIO OUTPUT ICI BIT ASSIGN.=	Decimal (0 thru 15) or hexadecimal ($0 thru $F) number of DDIO common output interrupt line A-register bit. Or N if an output ICI is not to be checked.
INPUT INTERRUPT ENABLED (Y OR N) =	Y for a direct interrupt. Or N for an I/O interrupt.
DDIO INPUT INT LINE=	Decimal (8 thru 15) or hexadecimal ($8 thru $F) number of interrupt-level (A-bus interrupt to processor).
DDIO INPUT ICI BIT ASSIGN.=	Decimal (0 thru 15) or hexadecimal ($0 thru $F) number of DDIO common input interrupt line A-register bit. Or N if an input ICI is not to be checked.

Table 6-1. TESDDIO Control Parameters (Sheet 2 of 2)

Control Parameter Request	Operator Input
ENTER HIGHEST GROUP (0-15) DOG GROUP=	Highest number of the output driver groups used.
DIG GROUP=	Highest number of the input driver groups used.

Table 6-2. TESDDIO SENSE Switch Settings

SENSE Switch	Position of Switch	
	Up (On)	Down (Off)
1	Error halt.*	Continue.
2	Suppress message printout. Suppresses both error message and test completion message printouts. Overrides SSW1 testing.	Enable error message printout (except $000A).
4**	Repeat test routine. If an error is detected, the program repeats the test to the point of error.	Continue.
8	Abort test in progress. The program returns to T2SEXC. RUN prints out.	Continue.

*The message is printed (except for error $000A) and the test continues after the processor RUN switch is pressed.
**Sense switch 4 has priority over the pass count feature if set prior to test completion. If set during BT test, the routine being executed will repeat.

Table 6-3. TESDDIO Subprograms

Subprogram	Test Identifier
Command Acceptance	CA
Group Selection	GS
Increment Group	IG
Move Bit	MB
Incrementing Pattern	IP
Basic Tests	BT
Intermediate Register Check	IR
Select Test Module Test	SM
Error Queuing	EQ

Table 6-4. TESDDIO Operating Interface Outputs (Sheet 1 of 2)

Test	Output	Action Required/Meaning
All	?	Invalid input. A valid input can be entered following the question mark.
CA	RUN ADDRESS CHECKING FEATURE (Y OR N)=	Enter Y, CR to cause an incremental advance of each address from 0 thru 63 performed by an RDS instruction. If a halt occurs, check A-Register for valid address. Enter N, CR to address DDIO only by the configured address.
MB, IP, BT	OUTPUT GROUP=	Enter digital output card (group) number (0 thru 15) to be tested, then CR.
	INPUT GROUP=	Enter digital input card (group) number (0 thru 15) to be tested, then CR.
	IS TEST CONNECTOR ON ? (Y OR N)	Connect test cable assembly (104208) between designated cards and enter Y, CR. Entering an N, CR causes the message to repeat until a Y is entered. Repeat test for each combination of input/output groups tested.
SM	OUTPUT GROUP=	Enter digital output card (group) number (0 thru 15) to be tested, then CR.
	INPUT GROUP=	Enter digital input card (group) number (0 thru 15) to be tested, then CR.

Table 6-4. TESDDIO Operating Interface Outputs (Sheet 2 of 2)

Test	Output	Action Required/Meaning
	IS TEST CONNECTOR ON ? (Y OR N)	Connect test cable assembly (104208) between designated cards and enter Y, CR. Entering an N, CR causes the message to repeat until a Y CR is entered.
	SELECT MODULES TEST=	Enter directive or GO (to repeat previous SM test), then CR.
	TEST=	Enter another directive. The TEST message is repeated for a total of 14 times, or until a CR is entered. Repeat test for each combination of input/output groups tested.
EQ	*NUMBER OF ERRORS DETECTED=$	Prints number of errors detected.
	*QUEUED ERRORS: I REG=	Prints two digit error codes up to a maximum of ten errors.

6.6 OPERATIONS OPTIONS

The following paragraphs describe optional operations that may be performed during testing to aid the operator in using the test program to his best advantage.

6.6.1 Control Parameter

Control parameters requested by the program may be entered via a pre-punched paper tape. This is accomplished using a feature of the T2SEXC program. The tape must contain the desired control parameters, each followed by a CR.

6.6.2 Halting on an Error

As shown in Table 6-3, SENSE switch 1 may be placed in the up position to cause the program to halt the test on detection of an error. If the program halts on an error, the processor control panel RUN switch must be pressed momentarily for an error message printout or to continue.

6.6.3 Suppressing Message Printout

TTY message printouts may be suppressed by setting SENSE switch 2 up (Table 6-3). This prevents all messages (including test completion) from being printed out on the TTY. The message suppression feature is especially useful when troubleshooting using an oscilloscope.

6.6.4 Repeating a Test Routine

As shown in Table 6-3, a test may be continuously repeated by setting SENSE switch 4 up. If an error is detected and SENSE switch 4 is up, the program repeats the test to the point of the error. If the test routine is divided into parts, only the part where the error was detected is repeated.

A test routine that is being executed repeatedly (SENSE switch 4 up) may be terminated by setting SENSE switch 4 down.

6.6.5 Aborting a Test

A test may be aborted at any time by setting SENSE switch 8 up. This causes the program to abort the test in progress, printout the number of test cycles (passes) completed and return to RUN.

NOTE: After the test has been aborted and the program returned to RUN, *set SENSE switch 8 down.*

6.6.6 Resumption of Testing

If SENSE switch 1 is up when a halt occurs, momentarily press the processor control panel RUN switch to continue.

When it is necessary to resume testing from a halt condition and SENSE switch 1 is down, press the processor control panel RESET switch, set P=$2 and press RUN. This returns the program to RUN.

NOTE: The program may also be returned to RUN *by typing* B2 *at the TTY.*

A test can now be selected and executed.

6.6.7 Reconfiguring a Test

To reconfigure a test, proceed as follows:

1. At the processor control panel, momentarily press HALT.
2. Momentarily press RESET.
3. Set P=$0.
4. Momentarily press RUN. The TTY prints out the first statement for defining the test program configuration. The test program can now be reconfigured.

Test reconfiguration can also be accomplished as follows:

1. When RUN prints out on the TTY, type an up arrow (↑). This directive returns control to T2SEXC and a left-arrow (←) prints out.
2. Type B0.

   The program prints out the first statement for defining the test program configuration. The test program can now be reconfigured.

6.6.8 Returning Program Control to T2SEXC

To return program control to T2SEXC, proceed as follows:

1. At the processor control panel, momentarily press HALT.
2. Momentarily press RESET.
3. Set P=$4.
4. Momentarily press RUN. The TTY prints out:

   EXECUTIVE READY
   ←

   The program is now under T2SEXC control.

6.7 ERROR INDICATIONS

When the test program detects an error, an error message may be printed out or the test may be stopped by an error halt, if these functions are enabled.

NOTE: Momentarily pressing the processor control panel RUN switch resumes testing beginning with the instruction following the one that failed.

When an error message prints out, the program continues on as if the error had not occurred, unless the error halt function is enabled. As a result, a single error may propagate a number of error indications.

Error halts are identified by processor I-Register contents. Error indications and fault isolation information are listed in Table 6-5, by error halt.

6.8 COMMON I/O LOGIC VERIFICATION

Successful completion of the tests given in the preceding paragraphs validates the operation of the Common I/O Logic. Instruction rejection in either test indicates a possible malfunction in the Common I/O Logic.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 1 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
$0001	**EDF CWD REJECTED** This instruction should be unconditionally accepted by the DDIOC if the correct address is used. **Probable Cause** • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches 4A to 4D not installed, incorrectly wired, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC. **Localization/Verification of Cause** On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check that signal ADDA- (3B-8) has the same timing pattern as STRB+. 3. Check EKOF+ (8C-3) for a pulse during STRB+. 4. Check EKO- (8C-4) for a pulse during STRB+.
$0002	**EDF RST REJECTED** This instruction should be unconditionally accepted by the DDIOC if the correct address is used. **Probable Cause** • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches 4A to 4D not installed, incorrectly jumpered, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 2 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
	Localization/Verification of Cause On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check that signal ADDA- (3B-8) has the same timing pattern as STRB+. 3. Check EDOF+ (8C-3) for a pulse during STRB+. 4. Check EKO- (8C-4) for a pulse during STRB+.
$0003	WTO CMD REJECTED This instruction should be unconditionally accepted by the DDIOC if the correct address is used. **Probable Cause** • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches 4A to 4D not installed, incorrectly jumpered, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC. **Localization/Verification of Cause** On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check that signal ADDB- (3C-8) has the same timing pattern as STRB+. 3. Check EDOF+ (8C-3) for a pulse during STRB+. 4. Check EKO- (8C-4) for a pulse during STRB+.
$0004	WTI CMD REJECTED This instruction should ba unconditionally accepted by the DDIOC if the correct address is used.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 3 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
	Probable Cause • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches 4A to 4D not installed, incorrectly jumpered, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC. **Localization/Verification of Cause** On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check that signal ADDA- (3B-8) has the same timing pattern as STRB+. 3. Check EDOF+ (8C-3) for a pulse during STRB+. 4. Check EKO- (8C-4) for a pulse during STRB+.
$0005	RDS CMD REJECTED This instruction should be unconditionally accepted by the DDIOC if the correct address is used. Probable Cause • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches 4A to 4D not installed, incorrectly jumpered, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC. **Localization/Verification of Cause** On the DDIOC: 1. Sync on STRB-1 (6C-8). 2. Check that signal ADDA- (3B-8) has the same timing pattern as STRB+. 3. Check EKOF+ (8C-3) for a pulse during STRB+.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 4 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
$0006	**ICI CMD REJECTED** This instruction should be accepted by the DDIOC if an interrupt is present and the correct address is used. Probable Cause • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • Interrupt address patches 4A to 4D not installed, incorrectly jumpered or damaged. • ICI patches 7B or 7C not installed, incorrectly wired, or damaged. • Failure of instruction decode or EKO logic circuits in DDIOC. Localization/Verification of Cause On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check IADDA- (3D-12) if IINT+ (input interrupt) has the same timing pattern as STRB+. 3. Check IADDB- (3D-10) if OINT+ (output interrupt) has the same timing pattern as STRB+. 4. Check EKOF+ (8C-3) for a pulse during STRB+. 5. Check EKO- (8C-4) for a pulse during STRB+.
$0007	**ICI ILLEGALLY ACCEPTED** This instruction was accepted without an interrupt present. Probable Cause • Incorrect jumpers, faulty installation, or damaged 7B and 7C ICI patches. Localization/Verification of Cause On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check ICI CMDA+ (2C-4) for same timing pattern as STRB+.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 5 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
	3. Check ICI CMDB+ (2B-4) for same timing pattern as STRB+. 4. Check both interrupt flip-flops at 4E-5 and 4E-9 to ensure they are both false. If either is true, check patch 7A for proper installation, miswiring, or damage. 5. Check EKOF+ (8C-3) for a pulse during STRB+. 6. Check EKO- (8C-4) for a pulse during STRB+.
$0008	EDF X ILLEGALLY ACCEPTED Or KFD X ILLEGALLY ACCEPTED Illegal commands are accepted during the CA subprogram test. The illegal command is denoted by an octal number from 0 to 7 (denoted by X in message). The command is the O field value on the instruction. Probable Cause • DDIO address patching faulty. • Some other system controller address patching faulty. • Address bus faulty. Localization/Verification of Cause On the DDIOC: 1. Sync on STRB+ (6C-8). 2. Check EKOF+ (8C-3) for negative level. If positive during STRB+ time, perform next step. 3. Check ADDA- (3B-8), ADDB- (3C-8), IALDA- (3D-12), and IADDB- (3D-6) for positive level during STRB+.
$0009	WTI7 REJECTED This instruction should be unconditionally accepted by the DDIOC if the correct address is used.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 6 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
	Probable Cause • The DDIOC is not connected to the processor I/O bus. • Power is not present at the DDIOC. • DDIOC address patches (4A to 4D) not installed, incorrectly wired, or damaged. • Failure of instruction decode or EKO logic in DDIOC. **Localization/Verification of Cause** 1. Sync on STRB+ (6C-8). 2. Check that signal ADDA- (3B-8) has the same timing pattern as STRB+. 3. Check EKOF+ (8C-3) for a pulse during STRB+. 4. Check EKO- (8C-4) for a pulse during STRB+.
$000A	No message printed Occurs in the address test portion of the CA subprogram test when the RDS command is accepted. The A-Register contains the device address that EKO'd the RDS command. This address must be operator verified to determine if it is valid (a device with that address is in the system). **Probable Cause** • This halt is a normal procedural step. A-Register addresses are compared with known addresses assigned to system units. For incorrect comparisons, follow the steps for localization/verification of cause. • Faulty address bus. • Same device including DDIO responding to invalid address. **Localization/Verification of Cause** On the DDIOC: 1. Sync on STRB (6C-8). 2. Check EKOF+ (8C-3) for negative level. If positive during STRB+ time, perform next step. 3. Check ADDA- (3B-8), ADDB- (3C-8). Both should be positive.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 7 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
$000B	INTERMEDIATE REG DATA ERROR SB: XXXX IS: YYYY A comparison of intermediate register (DDIOC) and output data buffers input and output data (WTI-7) indicates a trouble. SB data is read from A-Register, IS data from B-Register. Probable Cause In DDIOC: • Incorrect data entering register. • Faulty register. • Faulty multiplexer. External/interface or element: • I/O bus. Localization/Verification of Cause 1. Sync on OSEQ1- (6E-1). 2. Compare DBXX bits in buffer registers (pins 5, 9, 2, 12) 6E, 6F, 7E and 7F with SB bits on printout. 6E-5: ODB00 6E-9: ODB01 6E-2: ODB02 6E-12: ODB03 Connections/signals use same pattern for ODB04 to ODB07 for 6F, ODB08 to ODB11 for 7E, and ODB12 to ODB15 to 7F. If comparison is correct, sync on WTICMD+ (2F-5) and compare DIBXX bits at output of select logic (pins 4, 7, 9, 12) of 8H, 7H, 6K, and 6M. 8H-4: DIB00 6K-4: DIB08 8H-7: DIB01 6K-7: DIB09 8H-9: DIB02 6K-9: DIB10 8H-12: DIB03 6K-12: DIB11 6M-1: DIB04 7H-4: DIB12 6M-4: DIB05 7H-7: DIB13 6M-10: DIB06 7H-9: DIB14 6M-13: DIB07 7H-12: DIB15

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 8 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
$000C	**EXTRA ICI BITS RECEIVED** A check is made when an interrupt occurs and if any extra ICI bits are received an error occurs. The extra bits are in the A-Register with this halt. Probable Cause • DDIO ICI bit patches 7B and 7C incorrectly jumpered, improperly installed, or damaged. • Other units in system have faulty ICI patches. • Faulty interrupt bit. Localization/Verification of Cause On DDIOC: 1. Sync on STRB+ (6C-8). 2. Check INTA+ (5E-8) and INTB+ (5E-6). If DDIO is not addressed, both should be low. If DDIO is addressed, INTA+ or INTB+ goes high.
$000D	**UNEXPECTED INPUT INT RECEIVED** DDIO produced an unexpected input interrupt. At halt, A-Register contains data received and B-Register the status of device. Probable Cause • Input interrupt enable flip-flop set. Localization/Verification of Cause Check that flip-flop 5F-5 is false.
$000E	**UNEXPECTED OUTPUT INT RVCD** DDIO produced an unexpected output interrupt. At halt, A-Register contains data produced (zero) and B-Register the status of device. Probable Cause • Output interrupt enable flip-flop set. Localization/Verification of Cause Check that flip-flop 5F-9 is false.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 9 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
$0010	GROUP SELECTION ERROR SB XX IS YY A group was selected with an EDF CWD instruction. Result read by an RDS instruction. Comparison was not correct. SB group number is read from A-Register; IS group from B-Register. Probable Cause • Input/Output data bus malfunctioning. • DDIOC group address counter malfunctioning. • EDFLD- not at correct level. • DDIOC input select logic malfunctioning. Localization/Verification of Cause 1. Sync on EDFCMD+ (2C-1). 2. Check EDFLD- (2E-3) for same timing as EDFCMD- (2C-1). 3. Compare group address lines DOB12 to DOB15 at 5H-4, 10, 3, and 11 with address counter output at 5H-5, 9, 2, and 12 respectively. 4. Move sync to RDSCMD+ (8H-1). 5. Check that DIB12, 13, 14, and 15 pattern (7H-4, 7, 9, and 12) is the same as DOB12, 13, 14, and 15 (5H-11, 3, 10, and 4) during EDF Command (2A-1). 6. If step 5 is correct, check DIB12, 13, 14, and 15 for normal shifting onto the bus.
$0011	WTO INCREMENT ERROR SB: XX IS: YY A WTO instruction with an increment command did not advance the group address counter correctly. Status is read by an RDS instruction. Probable Cause • WTOIEN+ not in set state. • WTO increment enable flip-flop not in set state. • WTO sequence counter (SQF3+ and SQF4+) malfunctioning. • Group select counter (GSC0+ to GSC3+) malfunctioning.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 10 of 13)

Error Code Display For A-Register	Error Message and Troubleshooting Procedure
	Localization/Verification of Cause 1. Sync on WTOCMD+ (2B-1). 2. Check that a clock (GSCCK+) is produced at 4M-6 at the end of each WTOCMD+ timing signals.
$0012	**WTI INCREMENT ERROR SB: XX IS: YY** A WTI instruction with an increment command did not advance the group address counter correctly. Status is read by an RDS instruction. **Probable Cause** • If $0010 was not printed, check command decode logic. • WTIIEN+ increment enable flip-flop not in set state. • WTI sequence counter (SQF1+ and SQF2+) malfunctioning. • Group select counter (GSC0+ to GSC3+) malfunctioning. **Localization/Verification of Cause** 1. Sync on WTICMD+ (2B-10). 2. Check that a clock (GSCCK+) is produced at 4M-6 at the end of each WTICMD+ timing signals.
$0013	**MOVE BIT DATA ERROR** **SB: YYYY IS: XXXX** The data transferred by a WTO instruction does not match that received when a WTI instruction was executed. Integrity of system is checked. Assumes basic tests have been successfully performed. IS data is read from A-Register. SB data read from B-Register. **Probable Cause** • Faulty test connector. • Faulty digital input receiver or driver output PC board. • Faulty control section on transceiver/decoder PC board.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 11 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure

Localization/Verification of Cause

1. If there is another DDIOB digital output buffer PC board, swap with it. Repeat BT test. If trouble is corrected, first PC board is faulty. If trouble still remains, repeat for digital input receiver.

2. If only one card is used, sync on term OUT-6, of the DDIO Output Card (4A-5). Check data pattern at selected DDIOB digital output PC card drivers for an error using the following list:

Printout SB	Location	Signal
0001	2A-13	B15
0002	2A-12	B14
0004	2A-5	B13
0008	2A-4	B12
0010	2B-13	B11
0020	2B-12	B10
0040	2B-5	B09
0080	2B-4	B08
0100	3A-13	B07
020C	3A-12	B06
0400	3A-5	B05
0800	3A-4	B04
1000	3B-13	B03
2000	3B-12	B02
4000	3P-5	B01
8000	3B-4	B00

3. Check that selected digital output card address is negative during OUT-6. The address and location on the Transceiver card is as follows:

AD00 - 1A-1	AD08 - 1A-8
AD01 - 1A-2	AD09 - 1A-9
AD02 - 1A-3	AD10 - 1A-10
AD03 - 1A-4	AD11 - 1A-11

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 12 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure

AD04 - 1A-5 AD12 - 1A-12
AD05 - 1A-6 AD13 - 1A-13
AD06 - 1A-7 AD14 - 1A-14
AD07 - 1A-8 AD15 - 1A-15

If any errors exist, check transceiver/decoder logic.

4. Check that DCLK-1 (2B-8) on the transceiver card has a negative pulse during the last half of OUT-6.

5. Check data pattern at DDIOB digital output drivers on the output board. Driver signal and location below correspond to hexadecimal error printout in step 2 (UODOO=$8000).

UODOO - 3D-4 UOD08 - 2D-4
UOD01 - 3D-9 UOD09 - 2D-9
UOD02 - 3D-10 UOD10 - 2D-10
UOD03 - 1C-4 UOD11 - 1D-10
UOD04 - 3C-4 UOD12 - 2C-4
UOD05 - 3C-9 UOD13 - 2C-9
UOD06 - 3C-10 UOD14 - 2C-10
UOD07 - 1D-4 UOD15 - 1D-9

6. Sync on ISEQ at 2C-1 on transceiver/decoder. Check data pattern at DDIOB digital input receiver. Receiver signal and location below correspond to hexadecimal error printout in step 2 (UIDOO=$8000).

UIDOO - 2A-10 UID08 - 1A-10
UID01 - 2B-10 UID09 - 1B-10
UID02 - 2C-10 UID10 - 1C-10
UID03 - 2D-10 UID11 - 1D-10
UID04 - 2A-7 UID12 - 1A-7
UID05 - 2B-7 UID13 - 1B-7
UID06 - 2C-7 UID14 - 1C-7
UID07 - 2D-7 UID15 - 1D-7

7. If step 6 is normal, repeat step 3 for the selected digital input PC card.

Table 6-5. TESDDIO Error Display and Troubleshooting (Sheet 13 of 13)

Error Code Display For I-Register	Error Message and Troubleshooting Procedure
	8. If the above steps produce normal results, check DDIO bus at transceiver/decoder (DB00- thru DB15-). 9. Check that DCLK-1 (2B-8) is bracketed by syn pattern. 10. Check group select address decode at the following location on the transceiver decoder: GSC0 - P1-52 GSC1 - P1-53 GSC2 - P1-54 GSC3 - P1-55
$0014	INC PATTERN DATA ERROR SB: YYYY IS: XXXX The incrementing data pattern transferred by a WTO instruction does not match that received when a WTI instruction was executed. IS data is read from A-Register. SB data is read from B-Register. Probable Cause • Faulty cable terminator. • Faulty DDIOB digital output driver board. • Faulty DDIOC output data buffer. • Faulty power distribution. Localization/Verification of Cause Follow verification procedure described in error printout $0013.

APPENDIX A
INSTRUCTION SUMMARY

The table contained in this appendix provides a summary of all instructions accepted by the DDIO Subsystem hardware.

The tables include the following:

- Mnemonic and name, as referred to in text.
- Macro Assembler format.
- Machine language format.

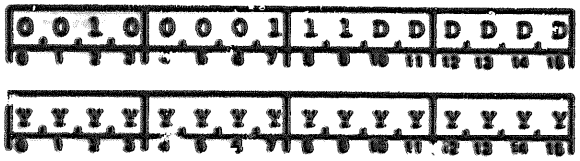
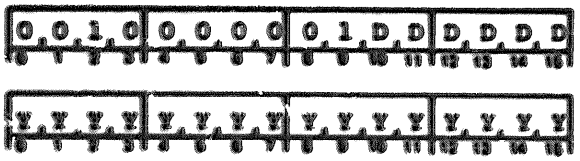
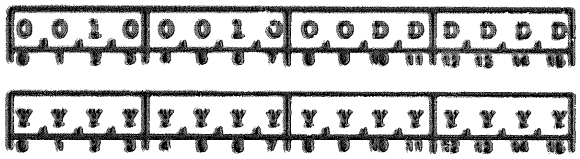
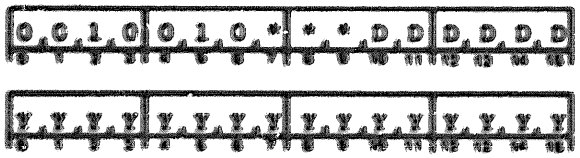
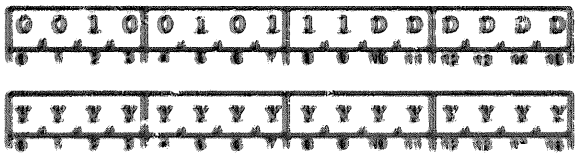
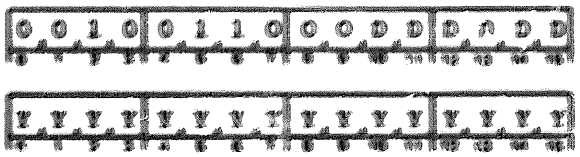
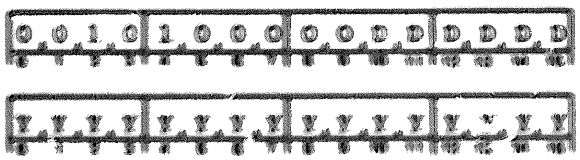
Conventions used in the tables are as follows:

DDDDDD = Address of controller(s) on the I/O bus to execute the command specified by OOO.

OOO = Order code (O field) of specific function to be performed, transmitted to the controller specified by DDDDDD.

Y = Address of branch on reject of instruction.

Table A-1. DDIO Controller Instructions

Mnemonic/ Name	Macro Assembler Format	Machine Language Format
EDF RST: Reset	EDF D,Y, 7	
EDF CMD: Command	EDF D,Y, 1	
WTO: Word Transfer Out	WTO D,Y,	
WTI: Word Transfer In	WTI D,Y, 0-6	 *Can be 000, 001, 010, 011, 100, 101, or 110.
WTI7	WTI D,Y, 7	
RDS: Request Device Status	RDS D,Y	
ICI: Interrogate Common Interrupts	ICI D,Y	

APPENDIX B
CONNECTOR PIN ASSIGNMENTS

The following tables list connector pin assignments for the various assemblies of the DDIO Subsystem:

Table	Connector
B-1	Internal I/O Bus Connector J1 (DDIOC).
B-2	Internal I/O Bus Connector J2 (DDIOC).
B-3	DDIOC Connector J11.
B-4	DDIOC Connector J12.
B-5	Power Backplane Connector P14.
B-6	DDIOB Transceiver/Decoder PC Board Connector J1.
B-7	DDIOB Transceiver/Decoder PC Board Connector J2.
B-8	DDIOB Transceiver/Decoder PC Board connector P1.
B-9	DDIOB Digital Output Driver PC Board Connector J1.
B-10	DDIOB Digital Output Driver PC Board Connector P1.
B-11	DDIOB Digital Input Receiver PC Board Conector J1.
B-12	DDIOB Digital Input Receiver PC Board Connector P1.

Table B-1. Internal I/O Bus Connector J1 Pin Assignments (DDIOC)

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
DIBC6-	01	DIB05-	14	GROUND	27	INT14-	40
DIB14-	02	DIB08-	15	INT13-	28	GROUND	41
DIB04-	03	DIB09-	16	GROUND	29	SPARE	42
DIB01-	04	GROUND	17	INT12-	30	GROUND	43
DIB00-	05	EKO-	18	GROUND	31	PCLK-	44
DIB15-	06	GROUND	19	INT08-	32	GROUND	45
DIB12-	07	STRB-	20	GROUND	33	DA05-	46
DIB13-	08	GROUND	21	INT10-	34	OF2-	47
DIB10-	09	SPARE	22	GROUND	35	OFO-	48
DIB11-	10	GROUND	23	INT11-	36	DA01-	49
DIB07-	11	INT15-	24	GROUND	37	OF1-	50
DIB02-	12	GROUND	25	INT09-	38		
DIB0	13	SPARE	26	GROUND	39		

Table B-2. Internal I/O Bus Connector J2 Pin Assignments (DDIOC)

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	DOB04-	14	SPARE	27	SPARE	40
GROUND	02	DOB05-	15	GROUND	28	SPARE	41
SPARE	03	DOB06-	16	SPARE	29	SPARE	42
GROUND	04	DOB01-	17	SPARE	30	GROUND	43
STRB-	05	DOB02-	18	GROUND	31	DA00-	44
GROUND	06	DOB00-	19	SPARE	32	DA02-	45
SPARE	07	DOB09-	20	GROUND	33	DA03-	46
GROUND	08	DOB03-	21	SPARE	34	DA04-	47
SPARE	09	DOB10-	22	GROUND	35	KF0-	48
DOB11-	10	DOB14-	23	SPARE	36	KF1-	49
DOB13-	11	DOB08-	24	GROUND	37	KF2-	50
DOB12-	12	DOB15-	25	SPARE	38		
DOB07-	13	GROUND	26	GROUND	39		

Table B-3. DDIOC Connector J1 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	GROUND	09	GROUND	17	DB13-	25
DB02-	02	DB00-	10	DB14-	18	DB12-	26
GROUND	03	GROUND	11	SPARE	19	GROUND	27
DB03-	04	DB01-	12	DB11-	20	DB07-	28
GROUND	05	SPARE	13	GROUND	21	GROUND	29
DB02-	06	DB08-	14	DB05-	22	DB06-	30
SPARE	07	GROUND	15	GROUND	23		
DB10-	08	DB11-	16	DB04-	24		

Table B-4. DDIOC Connector J12 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	GROUND	09	GROUND	17	SPARE	25
SPARE	02	SPARE	10	BII-	18	RST-	26
GROUND	03	GROUND	11	SPARE	19	GROUND	27
SPARE	04	ISBQA-	12	OUT-	20	DCLK-	28
GROUND	05	SPARE	13	GROUND	21	GROUND	29
SPARE	06	GSC0-	14	GSC3-	22	BOI-	30
SPARE	07	GROUND	15	GROUND	23		
SPARE	08	GSC1-	16	GSC2-	24		

Table B-5. Power Backplane Connector J14 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
GROUND	01	PFR-	08	GROUND	A	60 HZ	J
GROUND	02	(Not Used)		GROUND	B	NOT USED	K
GROUND	03	MR-	09	GROUND	C	-12 VDC	L
GROUND	04	(Not Used)		GROUND	D	+12 VDC	M
+5 VDC	05	-12 VDC	10	+5 VDC	E	+12 VDC	N
+5 VDC	06	+12 VDC	11	+5 VDC	F		
+5 VDC	07	+12 VDC	12	+5 VDC	H		

Table B-6. DDIOB Traansceiver/Decoder PC Board Connector J1 Pin assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	GROUND	08	DCLK-	15	GSC2-	22
GROUND	02	GROUND	09	OUT-	16	GSC3-	23
GROUND	03	GROUND	10	ISBQ-	17	BOI-	24
GROUND	04	GROUND	11	SPARE	18	BII-	25
GROUND	05	GROUND	12	RST-	19		
GROUND	06	GROUND	13	GSC0-	20		
GROUND	07	SPARE	1	GSC1-	21		

Table B-7. DDIOB Traansceiver/Decoder PC Board Connector J2 Pin assignments.

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
GROUND	01	GROUND	1	[illegible]-	21	DB12-	11
GROUND	02	GROUND	[illegible]	[illegible]	22	DB06-	32
GROUND	3	GROUND	[illegible]	[illegible]	23	DB07-	33
GROUND	04	GROUND	[illegible]	[illegible]	24	DB14-	34
GROUND	05	GROUND	[illegible]	[illegible]	25	DB15-	35
GROUND	06	GROUND	[illegible]	[illegible]	26	SPARE	36
GROUND	07	GROUND	[illegible]	[illegible]	27	SPARE	37
GROUND	08	GROUND	[illegible]	[illegible]-	28		
GROUND	09	SPARE	[illegible]	DB [illegible]-	29		
GROUND	10	DB13-	20	DB00-	30		

Table B-8. DDIOB Transceiver/Decoder PC Board Connector P1 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	BO0	21	DCLK-	41	AD10-	61
GROUND	02	BO1	22	BO6	42	AD09-	62
SPARE	03	BO3	23	OI-	43	AD08-	63
GROUND	04	BO2	24	RST-	44	AD07-	64
SPARE	05	BO5	25	ISBQ-	45	AD06-	65
GROUND	06	BO4	26	II-	46	AD05-	66
DB13-	07	DB00-	27	BOI	47	AD04-	67
SPARE	08	DB05-	28	BII	48	AD03-	68
DB08-	09	DB03-	29	RST-	49	AD02-	69
DB09-	10	DB01-	30	DCLK-	50	AD01-	70
DB10-	11	DB06-	31	OUT-	51	AD00-	71
DB04-	12	DB02-	32	GSC0-	52	SPARE	72
DB11-	13	DB14-	33	GSC1-	53	SPARE	73
DB12-	14	DB07-	34	GSC2-	54	GROUND	74
BI1	15	BI5	35	GSC3-	55	+5V	75
BI2	16	DB15-	36	AD11-	56	GROUND	76
BO8	17	OUT-6	37	AD12-	57	+5V	77
BI0	18	BI4	38	AD15-	58	GROUND	78
BI3	19	BO7	39	AD14-	59	+5V	79
BO9	20	ISBQ-1	40	AD13-	60	SPARE	80

Table B-9. DDIOB Digital Output Driver PC Board Connector J1 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
DOD00	01	DOD08	11	GROUND	21	GROUND	31
DOD01	02	DOD09	12	GROUND	22	GROUND	32
DOD02	03	DOD10	13	GROUND	23	GROUND	33
SPARE	04	DOD11	14	GROUND	24	GROUND	34
DOD03	05	DOD12	15	GROUND	25	GROUND	35
DOD04	06	DOD13	16	GROUND	26	GROUND	36
DOD05	07	DOD14	17	GROUND	27	GROUND	37
SPARE	08	DOD15	18	GROUND	28		
DOD06	09	SPARE	19	GROUND	29		
DOD07	10	GROUND	20	GROUND	30		

Table B-10. DDIOB Digital Output Driver PC Board Connector Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	SPARE	21	SPARE	41	SPARE	61
GROUND	02	OUT-6	22	BO5	42	SPARE	62
SPARE	03	SPARE	23	SPARE	43	SPARE	63
GROUND	04	AD-	24	BO0	44	SPARE	64
-12V	05	SPARE	25	SPARE	45	SPARE	65
GROUND	06	B11	26	BO4	46	SPARE	66
SPARE	07	SPARE	27	SPARE	47	SPARE	67
SPARE	08	B15	28	BO1	48	SPARE	68
SPARE	09	SPARE	29	SPARE	49	SPARE	69
SPARE	10	B10	30	BO6	50	SPARE	70
SPARE	11	SPARE	31	SPARE	51	SPARE	71
SPARE	12	B14	32	BO2	52	+12V	72
SPARE	13	SPARE	33	SPARE	53	SPARE	73
SPARE	14	BO9	34	BO7	54	GROUND	74
SPARE	15	SPARE	35	SPARE	55	+5V	75
RST-1	16	B12	36	BO3	56	GROUND	76
SPARE	17	SPARE	37	SPARE	57	+5V	77
DCLK-1	18	BO8	38	SPARE	58	GROUND	78
SPARE	19	SPARE	39	SPARE	59	+5V	79
SPARE	20	B13	40	SPARE	60	SPARE	80

Table B-11. DDIOB Digital Input Receiver PC Board Connector J1 Pin Assignment

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
[illegible]	01	[illegible]	11	GROUND	21	GROUND	31
[illegible]	02	[illegible]	12	GROUND	22	GROUND	32
[illegible]	03	[illegible]	13	GROUND	23	GROUND	33
[illegible]	04	[illegible]	14	GROUND	24	GROUND	34
[illegible]	05	[illegible]	15	GROUND	25	GROUND	35
[illegible]	06	[illegible]	16	GROUND	26	GROUND	36
[illegible]	07	[illegible]	17	GROUND	27	GROUND	37
[illegible]	08	[illegible]	18	GROUND	28		
[illegible]	09	SPARE	19	GROUND	29		
[illegible]	10	GROUND	20	GROUND	30		

Table B-12. DDIOB Digital Input Receiver PC Board Connector P1 Pin Assignments

Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin	Signal Mnemonic	Pin
SPARE	01	SPARE	21	SPARE	41	SPARE	61
GROUND	02	SPARE	22	B05	42	SPARE	62
SPARE	03	SPARE	23	SPARE	43	SPARE	63
GROUND	04	SPARE	24	B00	44	SPARE	64
-12V	05	SPARE	25	SPARE	45	SPARE	65
GROUND	06	B11	26	B04	46	SPARE	66
SPARE	07	SPARE	27	SPARE	47	SPARE	67
SPARE	08	B15	28	B01	48	SPARE	68
SPARE	09	SPARE	29	SPARE	49	SPARE	69
SPARE	10	B10	30	B06	50	SPARE	70
SPARE	11	SPARE	31	SPARE	51	SPARE	71
SPARE	12	B14	32	B02	52	+12V	72
SPARE	13	SPARE	33	SPARE	53	SPARE	73
SPARE	14	B09	34	B07	54	GROUND	74
SPARE	15	SPARE	35	SPARE	55	+5V	75
SPARE	16	B12	36	B03	56	GROUND	76
SPARE	17	SPARE	37	SPARE	57	+5V	77
SPARE	18	A08	38	SPARE	58	GROUND	78
SPARE	19	SPARE	39	SPARE	59	+5V	79
CE-	20	B13	40	SPARE	60	SPARE	80

APPENDIX C

CABLE ASSEMBLIES

Wire lists for the cable assemblies used in the DDIO Subsystem are provided in the following tables:

Table	Cable Assembly
C-1	DDIO-to-Card File, Control (104198)
C-2	DDIO-to-Card File, Data (104199)
C-3	Communications System, Power (101596)

The DDIO Test Cable Assembly (104208) has wiring between connectors which corresponds pin for pin, i.e., pin 1 of connector P1 is wired to pin 1 of connector P2.

Table C-1. DDIO-to-Card File Control Cable Assembly (104198)

Wire No.	Signal Mnemonic	From	To	Wire No.	Signal Mnemonic	From	To
01	GROUND	P1-2	P2-27	11	GROUND	P1-8	P2-15
02	DCLK-	P1-15	P2-28	12	CSC1-	P1-21	P2-16
03	GROUND	P1-3	P2-21	13	GROUND	P1-9	P2-23
04	OUT-	P1-16	P2-20	14	CSC2-	P1-22	P2-24
05	GROUND	P1-4	P2-11	15	GROUND	P1-10	P2-21
06	IERQ-	P1-17	P2-12	16	CSC3-	P1-23	P2-22
07	GROUND	P1-6	P2-23	17	GROUND	P1-11	P2-29
08	RST-	P1-19	P2-26	18	EXI	P1-24	P2-30
09	GROUND	P1-7	P2-15	19	GROUND	P1-12	P2-17
10	CSC0-	P1-20	P2-14	20	EII-	P1-25	P2-14

Table C-2. DDIO-to-Card File Data Cable Assembly (104199)

Wire No.	Signal Mnemonic	From	To	Wire No.	Signal Mnemonic	From	To
01	GROUND	P1-01	P2-27	17	GROUND	P1-09	P2-11
02	DB13-	P1-20	P2-25	18	DB00-	P1-28	P2-10
03	GROUND	P1-02	P2-27	19	GROUND	P1-19	P2-11
04	DB12-	P1-21	P2-26	20	DB01-	P1-29	P2-12
05	GROUND	P1-03	P2-05	21	GROUND	P1-11	P2-05
06	DB09-	P1-22	P2-06	22	DB03-	P1-30	P2-04
07	GROUND	P1-04	P2-15	23	GROUND	P1-12	P2-03
08	DB08-	P1-23	P2-14	24	DB02-	P1-31	P2-02
09	GROUND	P1-05	P2-13	25	GROUND	P1-13	P2-29
10	DB04-	P1-24	P2-24	26	DB06-	P1-32	P2-30
11	GROUND	P1-06	P2-09	27	GROUND	P1-14	P2-25
12	DB10-	P1-25	P2-08	28	DB07-	P1-33	P2-26
13	GROUND	P1-07	P2-17	29	GROUND	P1-15	P2-17
14	DB11-	P1-26	P2-16	30	DB14-	P1-34	P2-18
15	GROUND	P1-08	P2-23	31	GROUND	P1-16	P2-21
16	DB05-	P1-27	P2-22	32	DB15-	P1-35	P2-20

Table C-3. Communications System Power Cable (101996)

Wire No.	Signal Mnemonic	From	To
01	+12 VDC	P1-1	BP-+12 1
02	CONFIG	P1-2	BP-GND A
03	COMMON	P1-3	BP-GND C
04	COMMON	P1-4	BP-GND B
05	COMMON	P1-5	BP-GND D
06	+5 VDC	P1-6	BP-+5V A
07	+5 VDC	P1-7	BP-+5V B
08	+5 VDC	P1-8	BP-+5V B
09	-12 VDC	P1-11	BP-NEG 1
10	+12 VDC	P1-12	BP POS 1
11	-12 VDC	P1-15	BP-NEG 1

APPENDIX D
LOGIC DIAGRAMS

The following logic diagrams are intended to be used as an aid to logic understanding and fault isolation:

Drawing Number	Title
300342	DDIO Logic Diagram
300346	DDIO Transceiver Logic Diagram
300341	DDIO Digital Input Board Logic Diagram
300345	DDIO Digital Output Board Logic Diagram

REV	E.O.NO.	DATE	DESCRIPTION	DWN	CKD	APP
X1	—	[illegible]	INITIAL RELEASE	S.S.	[illegible]	J.L.A.
X2	—	1-10-75	UPDATED SHT 2, SHT 6: ZONE 8A, ADDED [illegible]; SHT [illegible] ZONE [illegible] [illegible] — SHT 12 ZONE [illegible] ADDED 4F;	D.E.K.	[illegible]	[illegible]
Z	003110	1-30-75	SPECIAL PILOT RELEASE	D.T.	[illegible]	J.L.A.
A	003279	5-16-75	PRODUCTION RELEASE	S.B.	[illegible]	[illegible]

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.

3. ALL CAPACITOR VALUES ARE IN MICROFARADS.

2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W

1. REFERENCE DOCUMENTS:
   ASSEMBLY DWG - 104036
   TEST SPEC - 250740

NOTES: UNLESS OTHERWISE SPECIFIED

SPARE CIRCUITS		
GTE/IS P/N	REF. DES	NO. AVAIL
800000	2M	1
800003	2K	2
800004	6D, 4L	6
800043	8C	1
800049	3F	1
800095	2C, 4F	3
RP 850096	2L	10

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
R5	
C23	

REV	A	A	A	A	A	A	A	A	A	A	A	A	A
SH	1	2	3	4	5	6	7	8	9	10	11	12	13

SHEET REVISION STATUS

TOLERANCES [illegible]
REMOVE BURRS AND BREAK SHARP EDGES

FINISH — MATERIAL —

DWN	S. Spiegel	[illegible]
CKD	[illegible]	[illegible]
APP	[illegible]	[illegible]
APP		
APP		
APP	[illegible]	[illegible]

PROPRIETARY INFORMATION

GTE INFORMATION SYSTEMS

CODE IDENT 52483

TITLE LOGIC DIAGRAM - DDIO

SCALE NONE

SHEET 1 OF 13

SIZE C

DWG. NO. 300342

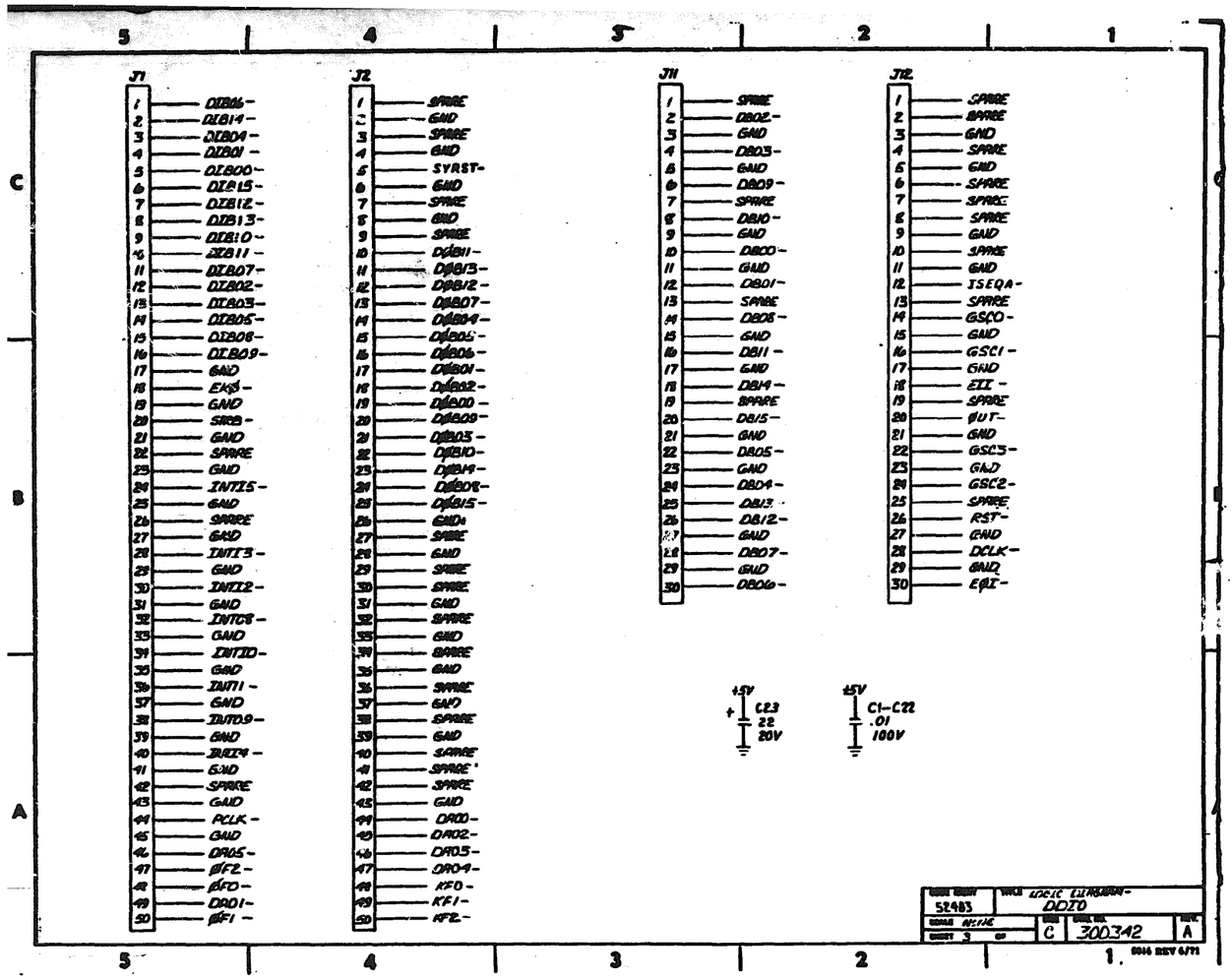
REV. A

D-4

	A	B	C	D	E	F	H	K	L	M	
8	800043 74H05	800043 74H05	800043 74H05	800015 74H04	SPARE	SPARE	800064 74157	800004 7404	800183 74S38	830095 TERM	8
7	PATCH	PATCH	PATCH	800004 7404	800051 74197	800051 74197	800064 74157	800004 7404	800183 74S38	830095 TERM	7
6	800004 7404	800004 7404	800004 7404	800004 7404	800651 74197	800051 74197	800183 74S38	800064 74157	800183 74S38	800095 7402	6
5	800004 7404	800004 7404	800043 74H05	800004 7404	800080 7408	800051 74197	800051 74197	SPARE	800183 74S38	830095 TERM	5
4	PATCH	PATCH	PATCH	PATCH	800049 7474	800095 7402	800000 7400	800080 7408	800004 7404	800183 74S38	4
3	SPARE	800006 7430	800006 7430	800003 7410	SPARE	800049 7474	800092 74107	800092 74107	800092 74107	SPARE	3
2	800096 7442	800095 7402	800095 7402	800096 7442	800000 7400	800080 7408	800095 7402	800003 7410	830096 PUP	800000 7400	2
1	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	SPARE	1
	A	B	C	D	E	F	H	K	L	M	

52483 LOGIC DIAGRAM - DDIO

SCALE NONE SHEET 2 C 300342 A


J1
1 DIB16-
2 DIB14-
3 DIB04-
4 DIB01-
5 DIB00-
6 DIB15-
7 DIB12-
8 DIB13-
9 DIB10-
10 DIB11-
11 DIB07-
12 DIB02-
13 DIB03-
14 DIB05-
15 DIB06-
16 DIB09-
17 GND
18 EXS-
19 GND
20 SRB-
21 GND
22 SPARE
23 GND
24 INTI5-
25 GND
26 SPARE
27 GND
28 INTI3-
29 GND
30 INTI2-
31 GND
32 INTI0-
33 GND
34 INTI0-
35 GND
36 INTI1-
37 GND
38 INTI0-
39 GND
40 INTI4-
41 GND
42 SPARE
43 GND
44 PCLK-
45 GND
46 DR05-
47 BIF2-
48 BIF0-
49 DR01-
50 BIF1-
J2
1 SPARE
2 GND
3 SPARE
4 GND
5 SYRST-
6 GND
7 SPARE
8 GND
9 SPARE
10 DIB11-
11 DIB13-
12 DIB12-
13 DIB07-
14 DIB04-
15 DIB05-
16 DIB06-
17 DIB01-
18 DIB02-
19 DIB00-
20 DIB09-
21 DIB03-
22 DIB10-
23 DIB14-
24 DIB08-
25 DIB15-
26 GND
27 SPARE
28 GND
29 SPARE
30 SPARE
31 GND
32 SPARE
33 GND
34 SPARE
35 GND
36 SPARE
37 GND
38 SPARE
39 GND
40 SPARE
41 SPARE
42 SPARE
43 GND
44 DR00-
45 DR02-
46 DR05-
47 DR04-
48 KF0-
49 KF1-
50 KF2-
J11
1 SPARE
2 DB02-
3 GND
4 DB03-
5 GND
6 DB09-
7 SPARE
8 DB10-
9 GND
10 DB00-
11 GND
12 DB01-
13 SPARE
14 DB08-
15 GND
16 DB11-
17 GND
18 DB14-
19 SPARE
20 DB15-
21 GND
22 DB05-
23 GND
24 DB04-
25 DB13-
26 DB12-
27 GND
28 DB07-
29 GND
30 DB06-
J12
1 SPARE
2 SPARE
3 GND
4 SPARE
5 GND
6 SPARE
7 SPARE
8 SPARE
9 GND
10 SPARE
11 GND
12 ISEQA-
13 SPARE
14 GSC0-
15 GND
16 GSC1-
17 GND
18 EII-
19 SPARE
20 BUT-
21 GND
22 GSC3-
23 GND
24 GSC2-
25 SPARE
26 RST-
27 GND
28 DCLK-
29 GND
30 EBI-
+5V
C23
22
20V
+5V
C1-C22
.01
100V
5
4
3
2
1
A
B
C
D
LOGIC DIAGRAM-
DDIO
52483
C
300342
A

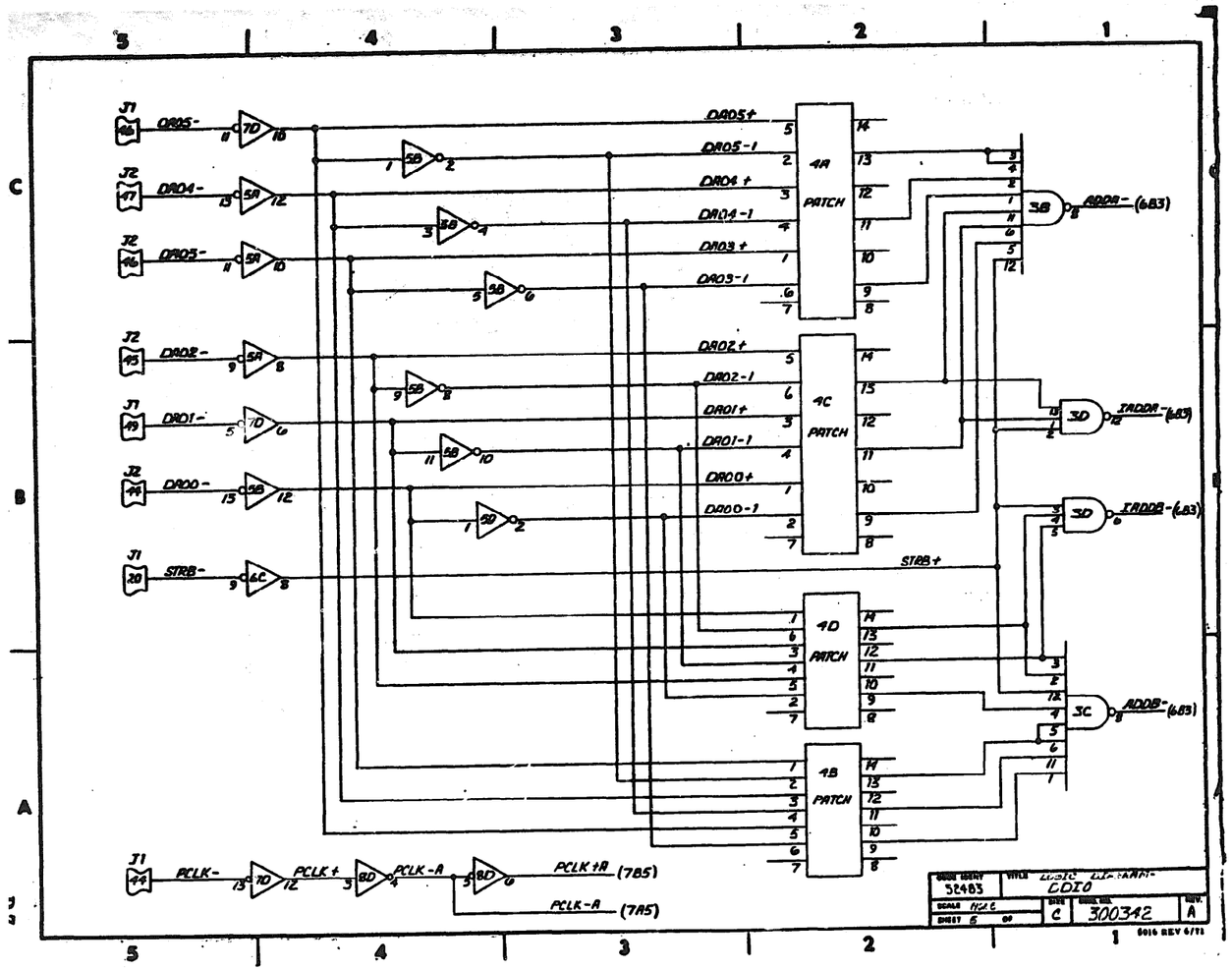
MNEMONIC GLOSSARY

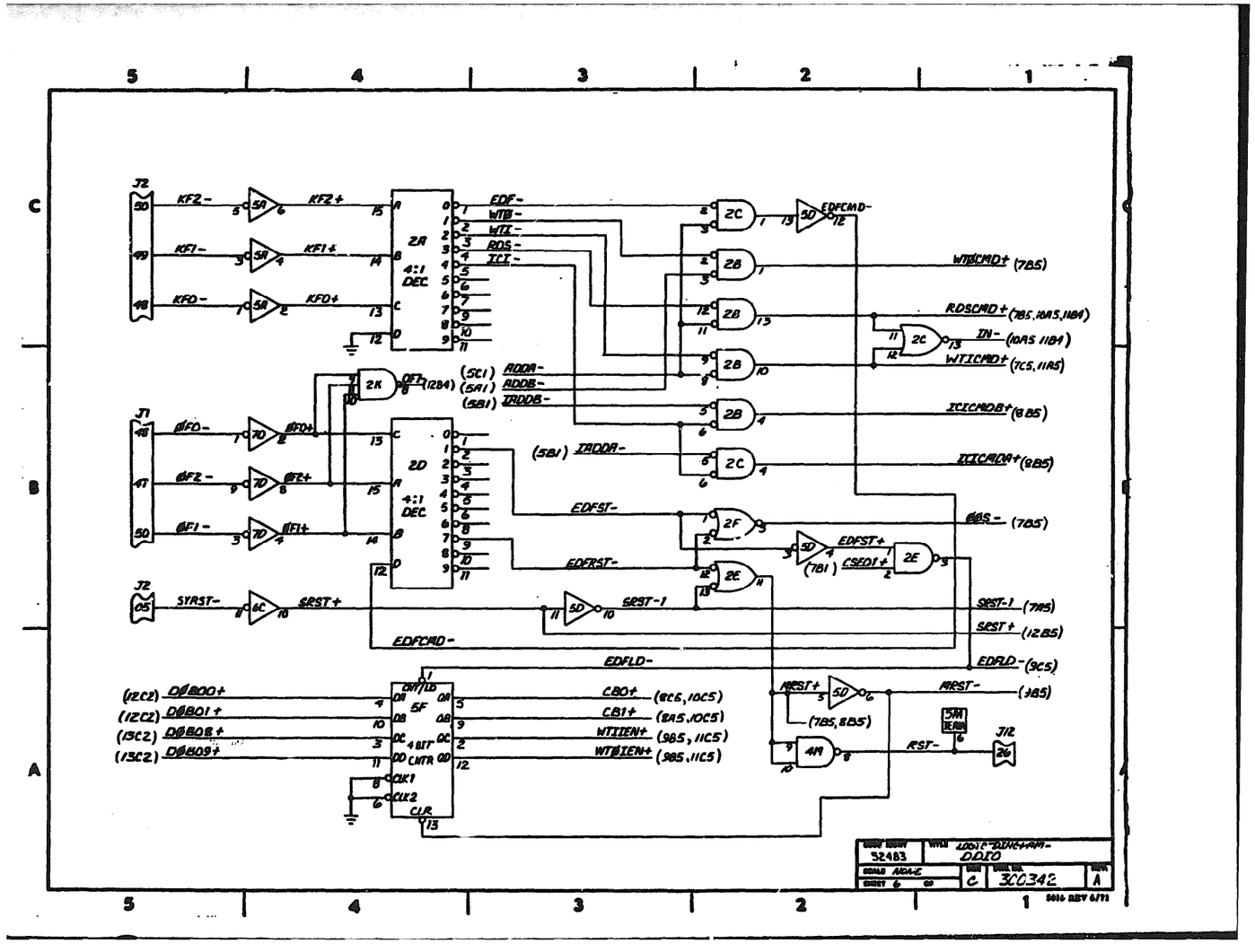
MNEMONIC	SOURCE	DEFINITION
ADD A,B	5A1,5C1	CONTROLLER ADDRESS
CBØ,1	6A3	INTERRUPT ENABLE FLIP-FLOPS
CIA,B	8A1,8B1	COMMON INTERRUPT A,B
CSEQ1	7B1	CONTROL SEQUENCE 1
DAØ-5	5B5,5C5	DEVICE ADDRESS
DB00-15	12,13	DATA BUS TO CARD FILE
DCLK	7C1	CLOCK TO CARD FILE
DIB00-15	8A1,8B1	DATA INPUT BUS
DØB00-15	12,13	DATA OUTPUT BUS
EDF	6C3	EXECUTE DEVICE FUNCTION
EDFCMD	6C2	EDF COMMAND DECODE
EDFLD	6B1	EDF LOAD
EDFRST	6B3	EDF RESET
EDFST	6B3	EDF START
EII	8C5	EXTERNAL INPUT INTERRUPT
EKØ	7A3	RESPONSE TO CPU
EKØFD	7A4	SET LOGIC TO EKØF
EKØF	7A4	EKØ FLIP-FLOP
EØI	8B5	EXTERNAL OUTPUT INTERRUPT
GSC0-3	9B2	GROUP SELECT COUNTER
GSCCK	9B4	GROUP SELECT COUNTER CLOCK
IADDA,B	5B1	ICI ADDRESS A,B
ICI	6C3	INTERROGATE COMMON INTERRUPT
ICICMDA,B	6B1	ICI COMMAND A,B
IDB00-15	10,11	INPUT DATA BUS
IINT	8C3	INPUT INTERRUPT
IN	6C1	INPUT DATA TIME
INT[illegible]5	8C2	INTERRUPT LINES TO CPU
INT A,B	8B3	INTERRUPT A,B
ISEQA	7C1	ALL INPUT SEQUENCES
ISEQ 1,2,3	7C1,7C2	INPUT SEQUENCE 1,2,3

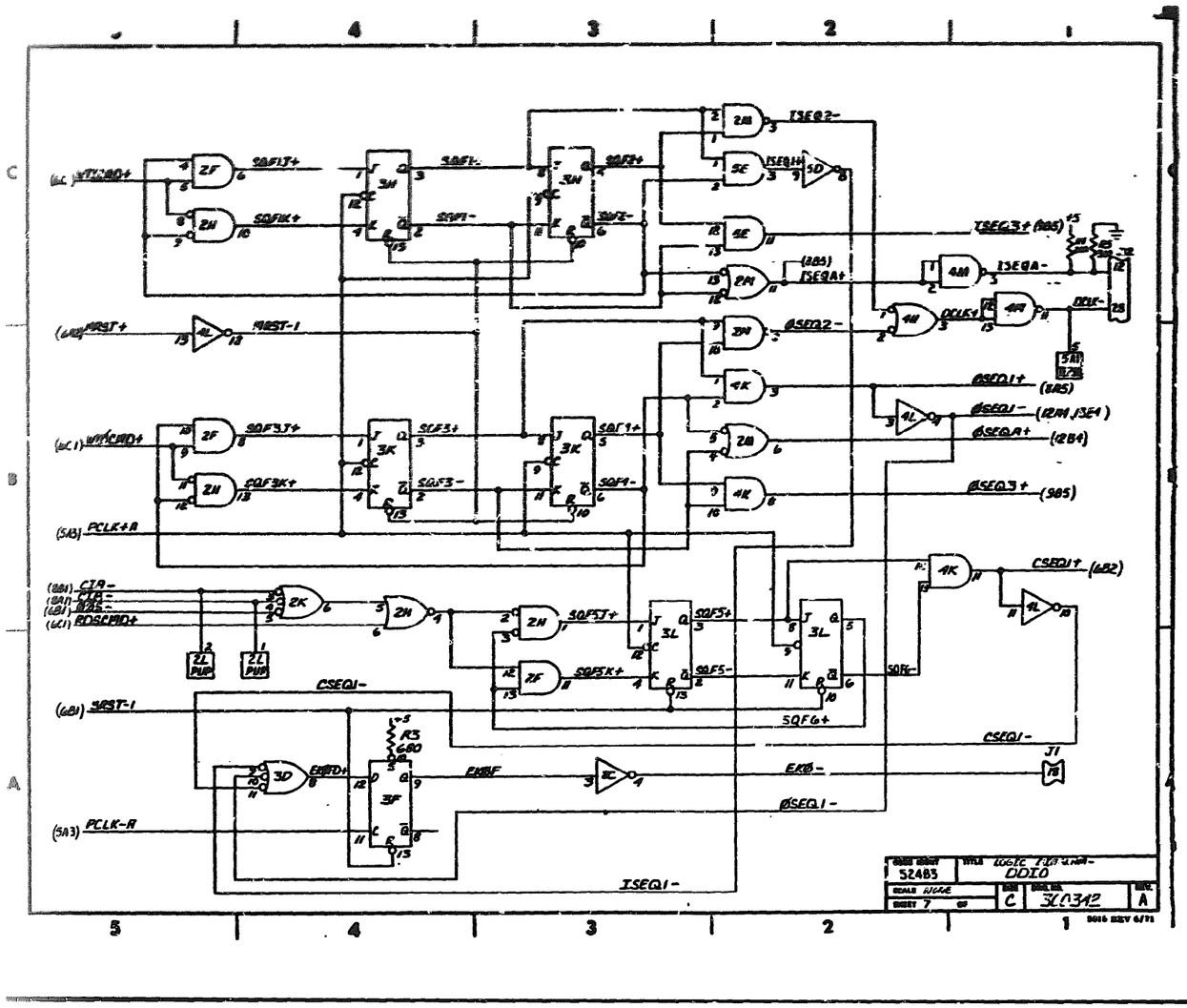
MNEMONIC GLOSSARY

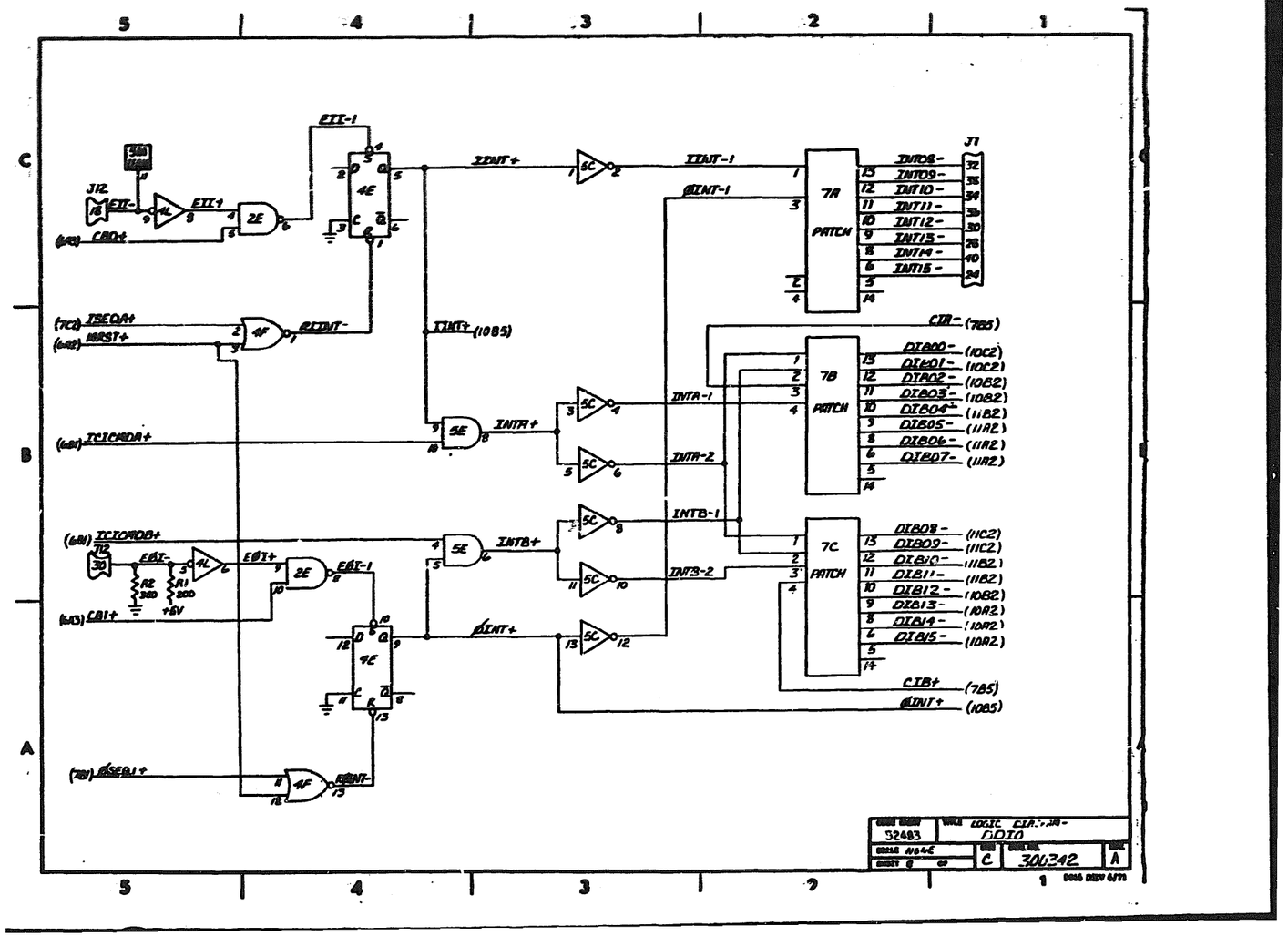
MNEMONIC	SOURCE	DEFINITION
KF0,1,2	6C4	COMMAND FIELD FROM CPU
MRST	6A2	MASTER RESET
ØDB00-15	12,13	OUTPUT DATA BUFFER
ØF0,1,2	6B4	ORDER FIELD FROM CPU
ØINT	8A4	OUTPUT INTERRUPT
ØØS	6B1	ONE OR SEVEN
ØSEQA	7B1	ALL OUTPUT SEQUENCES
ØSEQ 1,2,3	7B1,7B2	OUTPUT SEQUENCE
ØUT	13B2	OUTPUT TIME TO CARD FILE
PCLK	5A3	P CLOCK
RDS	6C3	REQUEST DEVICE STATUS
RDSCMD	6C1	RDS COMMAND
RIINT	8B4	RESET INPUT INTERRUPT
RØINT	8A4	RESET OUTPUT INTERRUPT
RST	6A1	RESET CARD FILE
SQF1-6	7	SEQUENCE FLIP-FLOPS
SRST	6B4	SYSTEM RESET
STRB	6B5	STROBE
WTI	6C3	WORD TRANSFER IN
WTICMD	6C1	WTI COMMAND
WTIIEN	6A3	WTI INCREMENT ENABLE
WTØ	6C3	WORD TRANSFER OUT
WTØCMD	6C1	WTØ COMMAND
WTØIEN	6A3	WTØ INCREMENT ENABLE

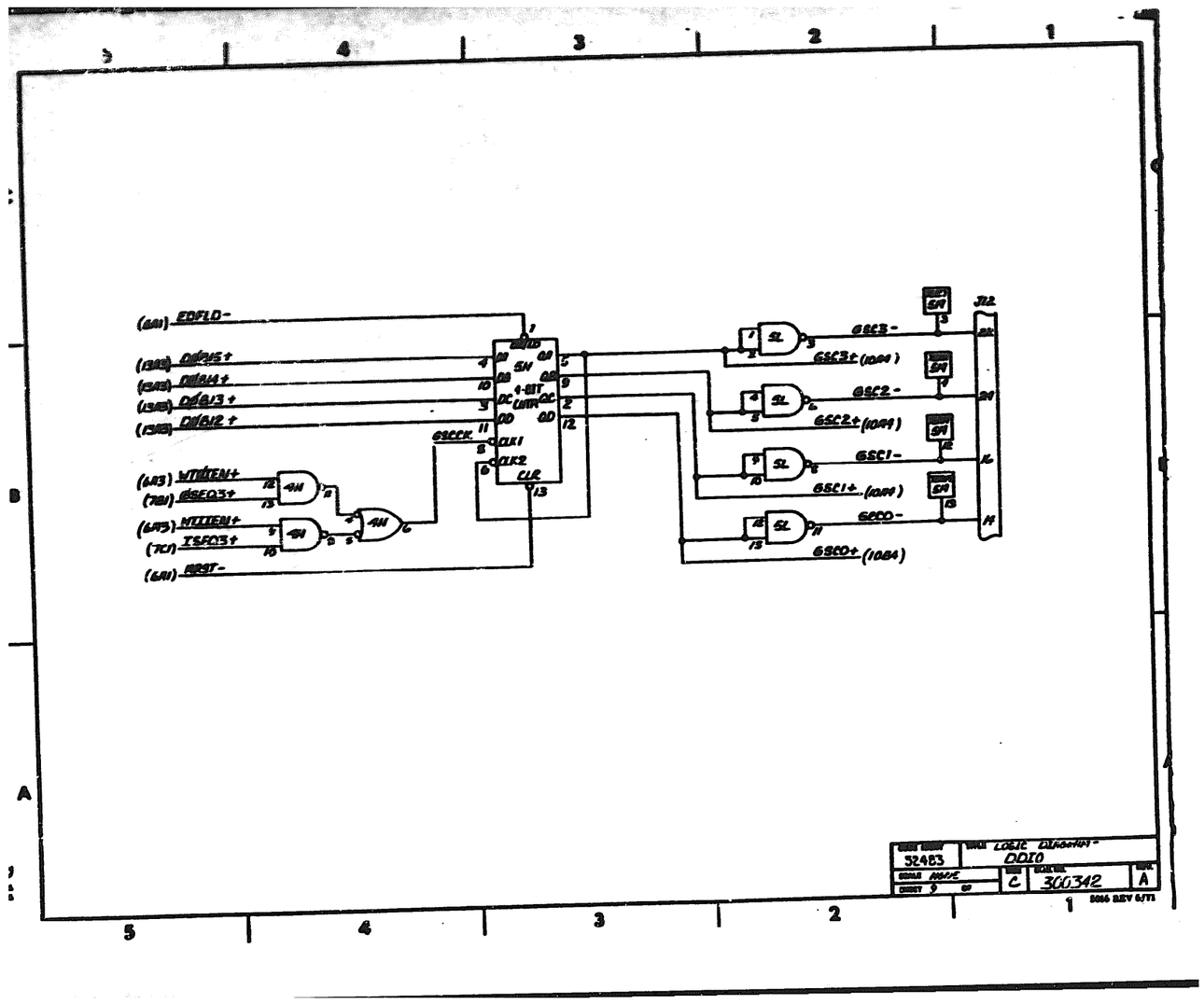
32483	LOGIC DIAGRAM - DDIO		
SCALE NONE	C	300342	A
SHEET 4 OF			

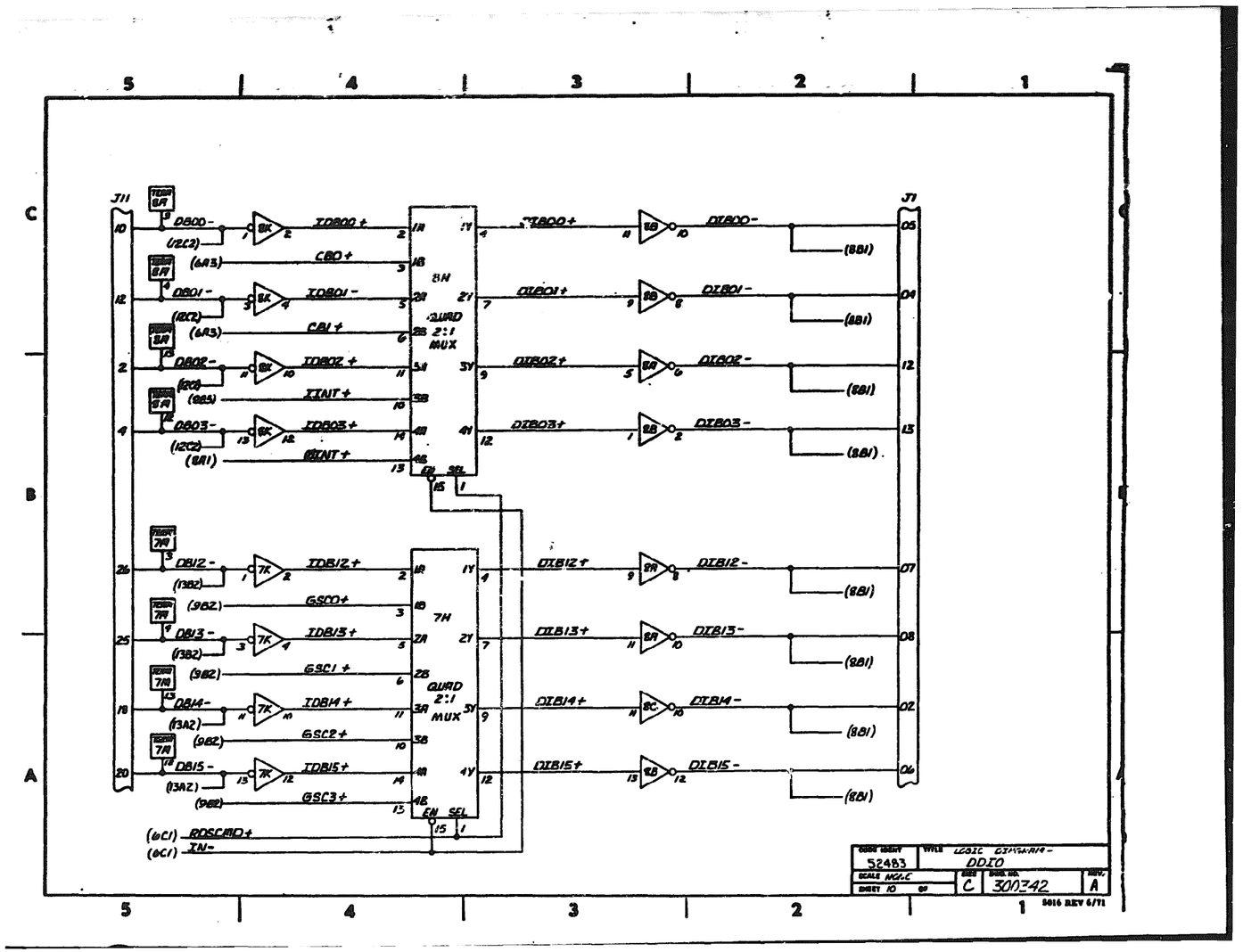

J1
J2
DA05-
DA04-
DA03-
DA02-
DA01-
DA00-
STRB-
PCLK-
DA05+
DA05-1
DA04+
DA04-1
DA03+
DA03-1
DA02+
DA02-1
DA01+
DA01-1
DA00+
DA00-1
STRB+
4A PATCH
4C PATCH
4D PATCH
4B PATCH
3B
3D
3C
ADDA- (6B3)
IADDA- (6B3)
ADDB- (6B3)
PCLK+A (7B5)
PCLK-A (7A5)
CDIO
300342

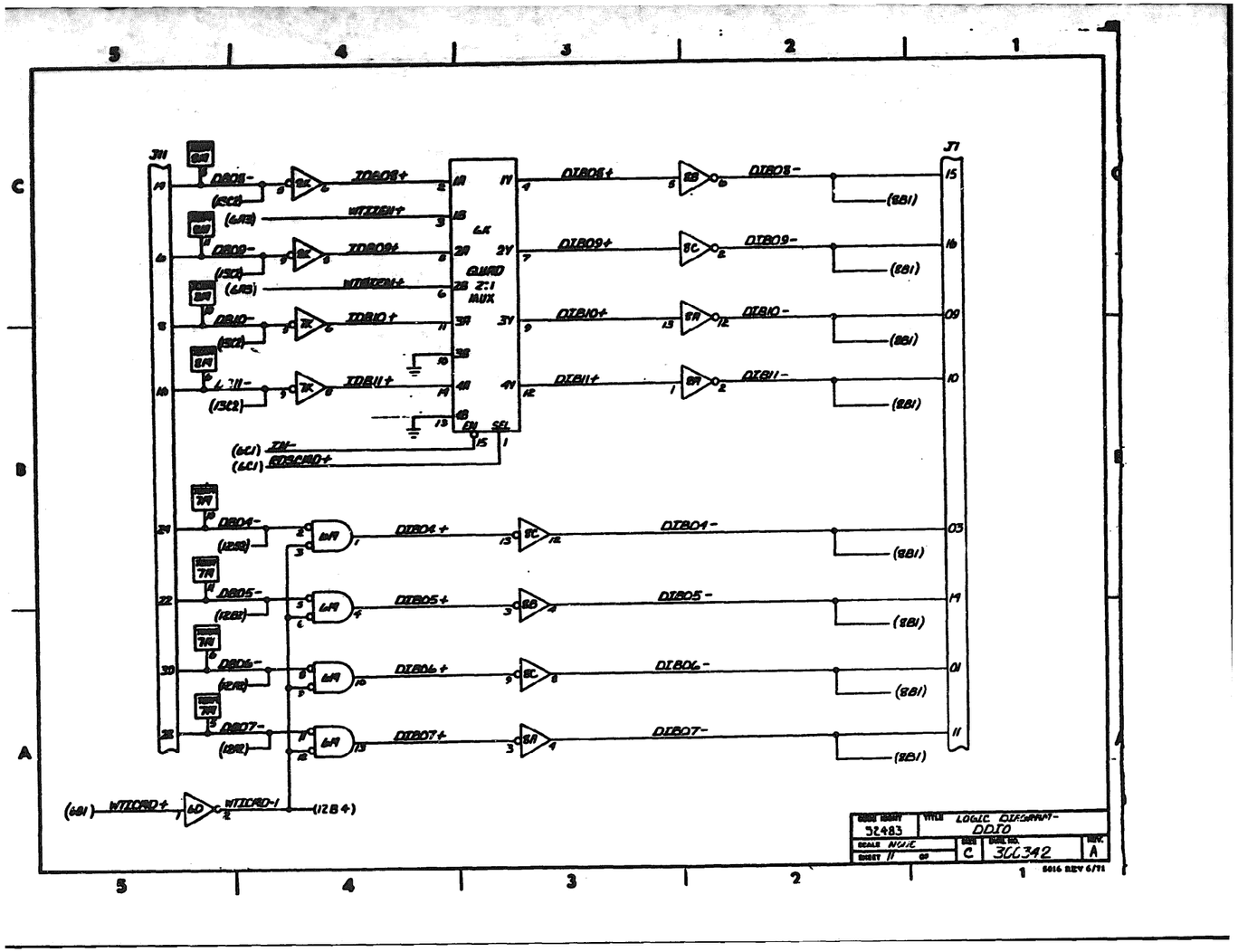

5
4
3
2
1
C
B
A
J2
KF2-
KF2+
KF1-
KF1+
KFD-
KFD+
2A
4:1 DEC
EDF-
WTB-
WTI-
RDS-
ICI-
2C
EDFCMD-
WTBCMD+ (7B5)
RDSCMD+ (7B5, 10A5, 11B4)
IN- (10A5 11B4)
WTICMD+ (7C5, 11A5)
ICICMDB+ (8B5)
ICICMDA+ (8B5)
EDFST-
EDFRST-
EDFST+
CSED1+
(7B1)
BRS- (7B5)
SRST-1 (7B5)
SRST+ (12B5)
EDFLD- (9C5)
EDFCMD-
EDFLD-
J1
ØFD-
ØFZ-
ØF1-
ØFD+
ØFZ+
ØF1+
2D
4:1 DEC
(5C1) ADDA-
(5A1) ADDB-
(5B1) IRADDB-
(5B1) IRADDA-
SYRST-
SRST+
SRST-1
(12C2) DØB00+
(12C2) DØB01+
(13C2) DØB08+
(13C2) DØB09+
5F
4 BIT CNTR
CBO+ (8C6, 10C5)
CB1+ (8A5, 10C5)
WTIIEN+ (9B5, 11C5)
WTØIEN+ (9B5, 11C5)
MRST+
MRST-
(7B5, 8B5)
4M
RST-
J12
32483
DDIO
C
30342
A

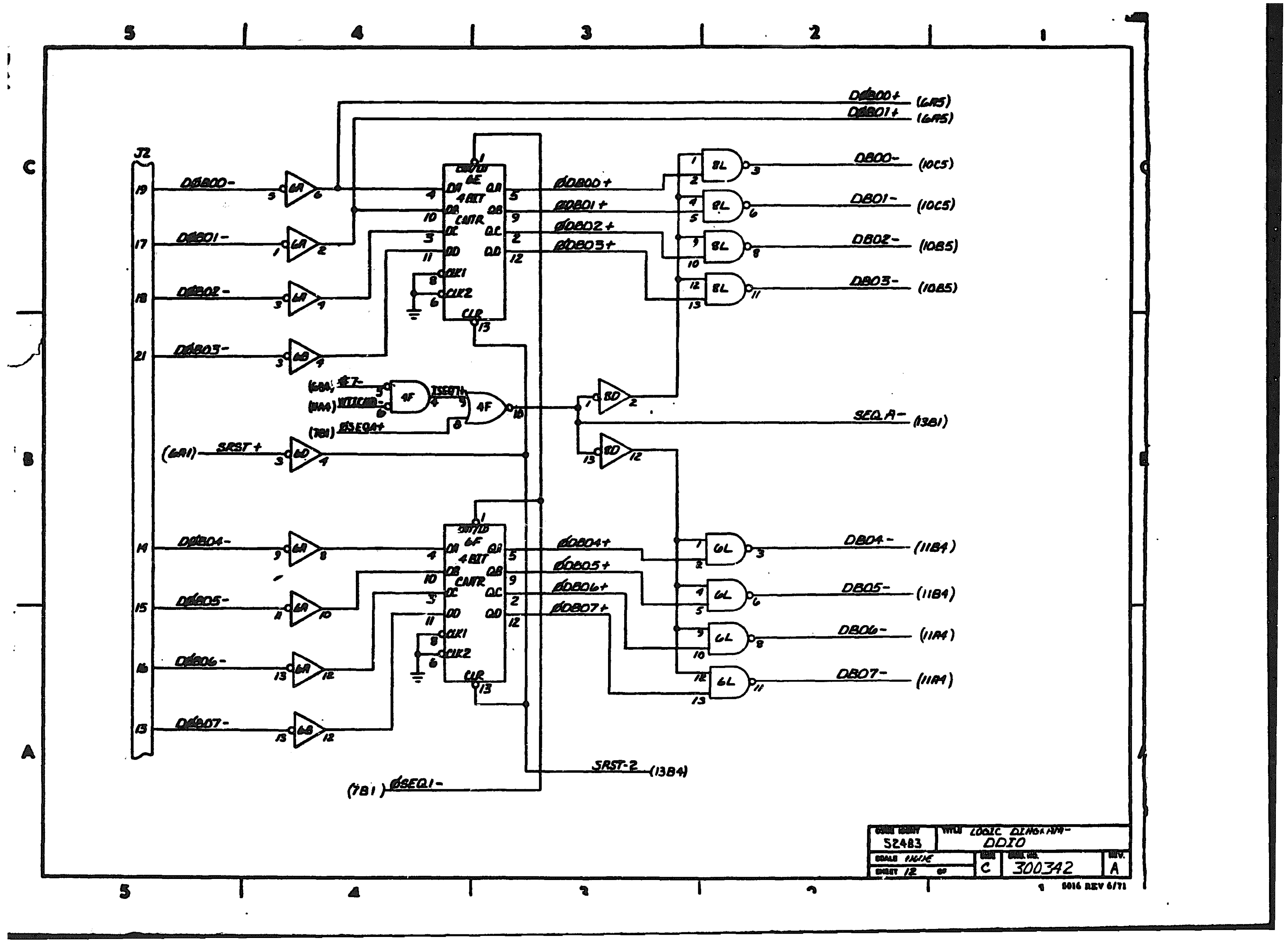

SQF13+
SQF1K+
SQF1-
SQF2+
SQF2-
ISEQ2-
ISEQ1+
ISEQ3+ (885)
ISEQA-
(885) ISEQA+
DCLK+
DCLK-
MRST+
MRST-1
ØSEQ2-
ØSEQ1+ (885)
ØSEQ1- (12M 13E4)
ØSEQA+ (12B4)
ØSEQ3+ (985)
SQF3J+
SQF3K+
SQF3-
SQF4-
PCLK+A
CTA-
CTB-
RDA-
RDSCMD+
SQF5J+
SQF5K+
SQF5-
SQF5+
SQF6+
CSEQ1+ (682)
CSEQ1-
SQF6-
MRST-1
R3 680
EKØF+
EKØF
EKØ-
ØSEQ1-
PCLK-A
ISEQ1-
J1
DDIO
52483
C
A

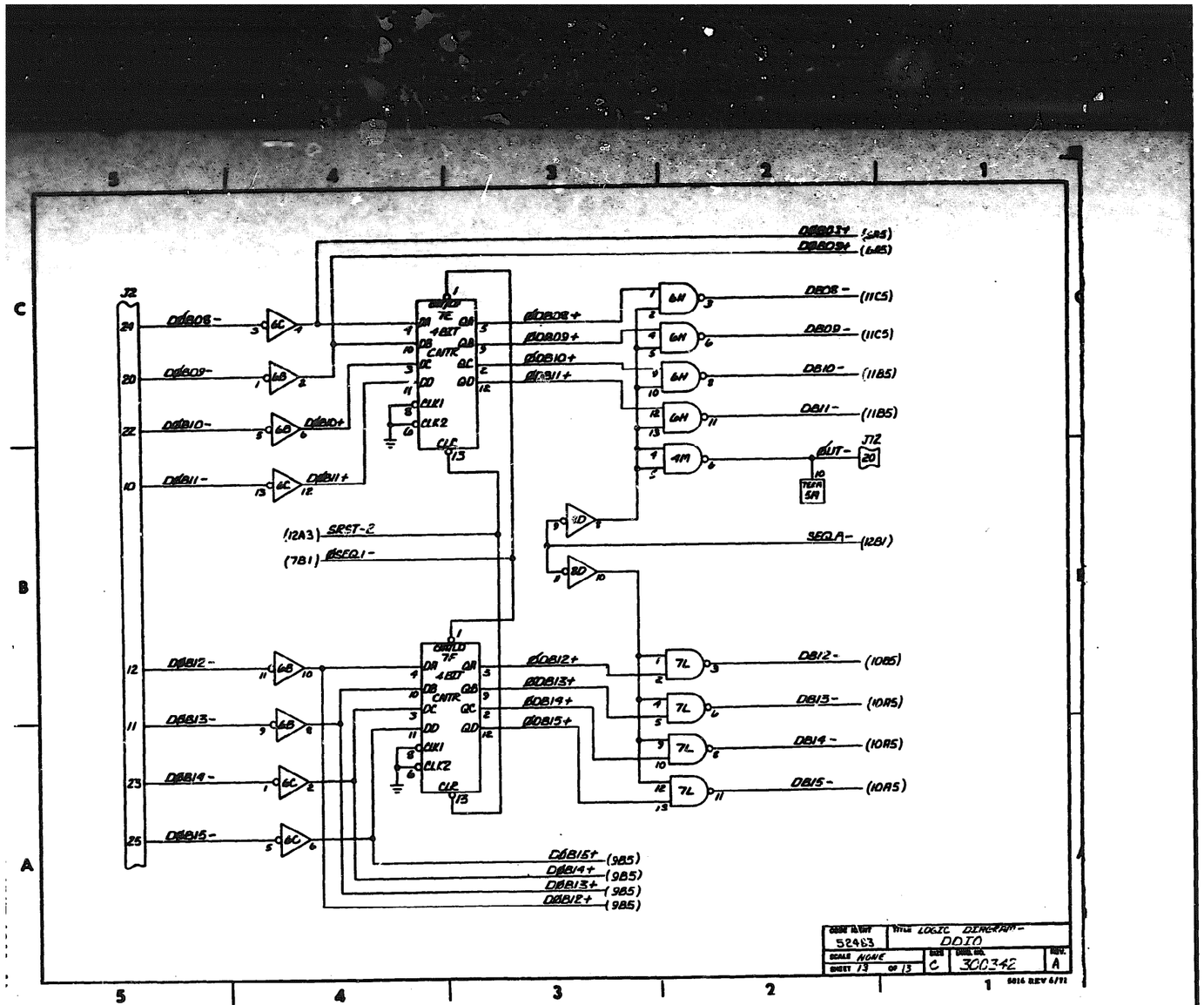

5
4
3
2
1
C
B
A
J12
EII-
EII+
CBOI+
2E
4E
EII-1
2EINT+
5C
IIINT-1
7A
PATCH
J1
INT08-
INT09-
INT10-
INT11-
INT12-
INT13-
INT14-
INT15-
(7C) ISEQA+
(6A3) MRST+
4F
ØEINT-
IINT+ (1085)
CIA- (785)
7B
DIB00- (10C2)
DIB01- (10C2)
DIB02- (10B2)
DIB03- (10B2)
DIB04- (11B2)
DIB05- (11A2)
DIB06- (11A2)
DIB07- (11A2)
5E
INTA+
INTA-1
INTA-2
(6A1) IOIOAOB+
EBI-
EØI+
EBI-1
R2 360
R1 200
+5V
(6A3) CBI+
INTB+
INTB-1
INT3-2
7C
DIB08- (11C2)
DIB09- (11C2)
DIB10- (11B2)
DIB11- (11B2)
DIB12- (10B2)
DIB13- (10A2)
DIB14- (10A2)
DIB15- (10A2)
ØINT+
CIB+ (785)
ØINT+ (1085)
(7B1) ØSEØI+
ØEINT-
32483
LOGIC CIA-,IA-
DDIO
C
30342
A


(6A11) EDFLD-
(5A8) DATA15+
(5A10) DATA14+
(5A12) DATA13+
(5A13) DATA12+
(6A13) WTTIEN+
(7B11) GSEC03+
(6A15) WTTIEN+
(7C1) ISEC03+
(6A11) MRST-
GSCCK
GSC3-
GSC3+ (1084)
GSC2-
GSC2+ (1084)
GSC1-
GSC1+ (1084)
GSC0-
GSC0+ (1084)
J12
32483
LOGIC EXPANSION - DD10
C
300342
A
SIZE
DRAWING NO.
REV
SHEET 9 OF
5016 REV 6/71


J11
J1
8N
2UARD 2:1 MUX
7H
QUARD 2:1 MUX
DB00-
DB01-
DB02-
DB03-
DB12-
DB13-
DB14-
DB15-
IDB00+
IDB01-
IDB02+
IDB03+
IDB12+
IDB13+
IDB14+
IDB15+
DIB00-
DIB01-
DIB02-
DIB03-
DIB12-
DIB13-
DIB14-
DIB15-
CBO+
CBI+
XINT+
GSC0+
GSC1+
GSC2+
GSC3+
RDSCMD+
IN-
LOGIC DIAGRAM -
DDIO
52483
SCALE NONE
SHEET 10 OF
SIZE C
DWG. NO. 300742
REV. A
9016 REV 6/71


J11
J7
DB08-
DB09-
DB10-
DB11-
DB04-
DB05-
DB06-
DB07-
IDB08+
IDB09+
IDB10+
IDB11+
IDB04+
IDB05+
IDB06+
IDB07+
WTIDBH+
WTIDBL+
WTICRD+
WTICRD-1
DIB08+
DIB09+
DIB10+
DIB11+
DIB04+
DIB05+
DIB06+
DIB07+
DIB08-
DIB09-
DIB10-
DIB11-
DIB04-
DIB05-
DIB06-
DIB07-
(12B4)
(12B1)
LOGIC DIAGRAM-
DDIO
32483
300342
C
A
SCALE NONE
SHEET 11 OF
5016 REV 6/71


J2
DØB00-
DØB01-
DØB02-
DØB03-
DØB04-
DØB05-
DØB06-
DØB07-
ØDB00+
ØDB01+
ØDB02+
ØDB03+
ØDB04+
ØDB05+
ØDB06+
ØDB07+
DØB00+ (6A5)
DØB01+ (6A5)
DB00- (10C5)
DB01- (10C5)
DB02- (10B5)
DB03- (10B5)
DB04- (11B4)
DB05- (11B4)
DB06- (11A4)
DB07- (11A4)
SEQ.A- (13B1)
SRST+
SRST-2 (13B4)
(7B1) ØSEQ1-
(7B1) ØSEQA+
4 BIT CNTR
CLR
LOGIC DIAGRAM-DDIO
52483
300342
C
A
5016 REV 6/71


J12
DBB08-
DBB09-
DBB10-
DBB11-
DBB12-
DBB13-
DBB14-
DBB15-
DBB15+ (985)
DBB14+ (985)
DBB13+ (985)
DBB12+ (985)
DBB08+
DBB09+
DBB10+
DBB11+
(12A3) SRST-2
(7B1) SEQ.1-
DB08- (11C5)
DB09- (11C5)
DB10- (11B5)
DB11- (11B5)
OUT- J12 20
SEQ.A- (12B1)
DB12- (10B5)
DB13- (10A5)
DB14- (10A5)
DB15- (10A5)
CODE IDENT 52463
TITLE LOGIC DIAGRAM - DDIO
SCALE NONE
SHEET 13 OF 13
SIZE C
DWG. NO. 300342
REV. A
5016 REV 6/72

REV	ED. NO.	DATE	DESCRIPTION	
X1			[illegible] RELEASE	
X2	003110	[illegible]	SPECIAL [illegible] RELEASE	
A	003279	[illegible]	PRODUCTION RELEASE	

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W
1. REFERENCE DOCUMENTS:
   ASSEMBLY DWG - 104050
   TEST SPEC - 250740

SPARE CIRCUITS		
GTE/IS. P/N	REF. DES	NO. AVAIL
830095 (7804)	1D	6

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C7	

A	A	A	A
1	2	3	4

SHEET REVISION STATUS

TOLERANCES XX ± .020 XXX ± .010 ANGLES ± 1/2° HOLE DIA ± .003
REMOVE BURRS AND BREAK SHARP EDGES

FINISH | MATERIAL

DWN	S. SPICKER	
CKD		
APP		
APP		
APP		
APP	RAC	

PROPRIETARY INFORMATION

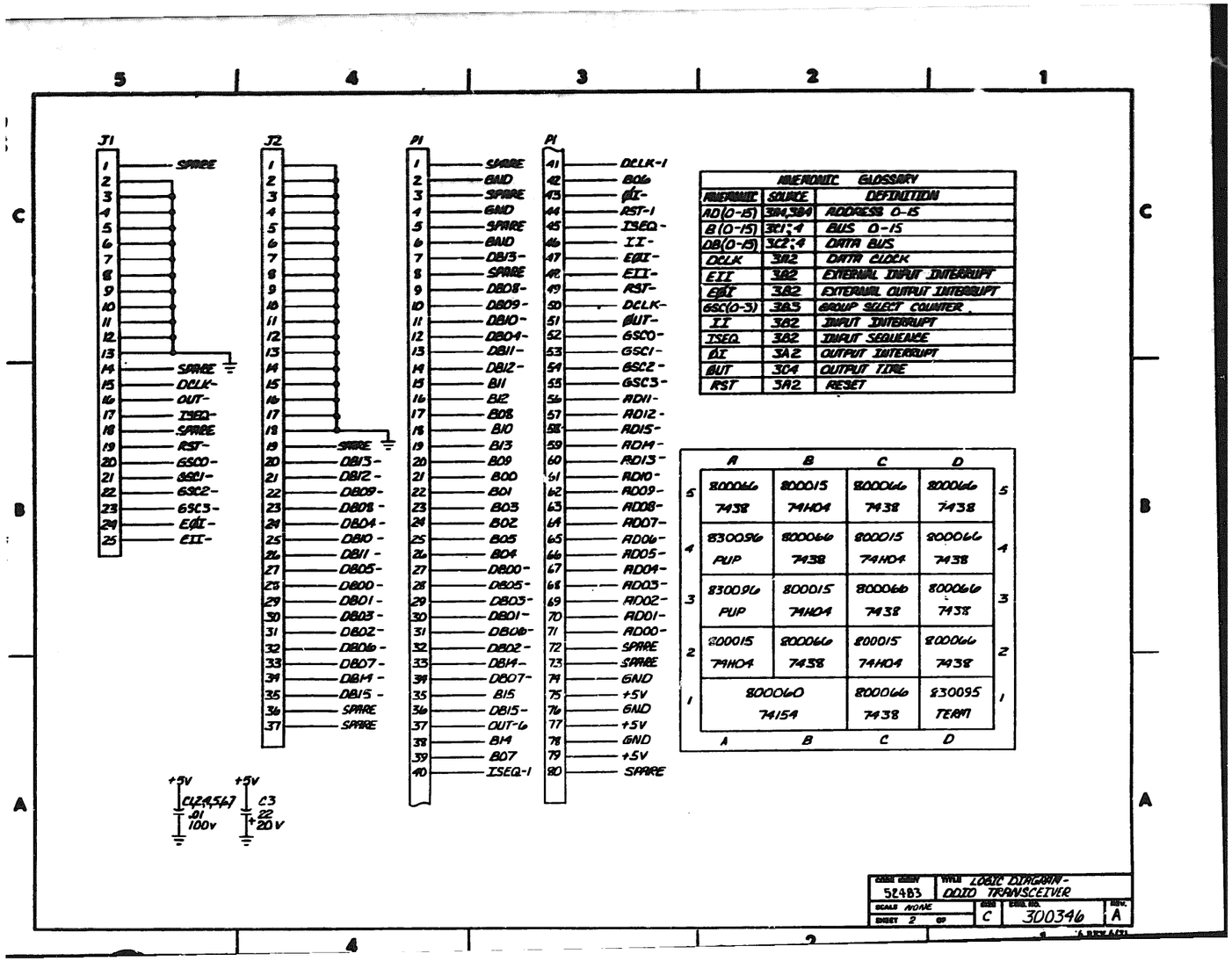
GTE INFORMATION SYSTEMS

CODE IDENT 52483

TITLE LOGIC DIAGRAM - DDIO TRANSCEIVER

SCALE NONE | SIZE C | DWG. NO. 300346 | REV. A

SHEET 1 OF 4

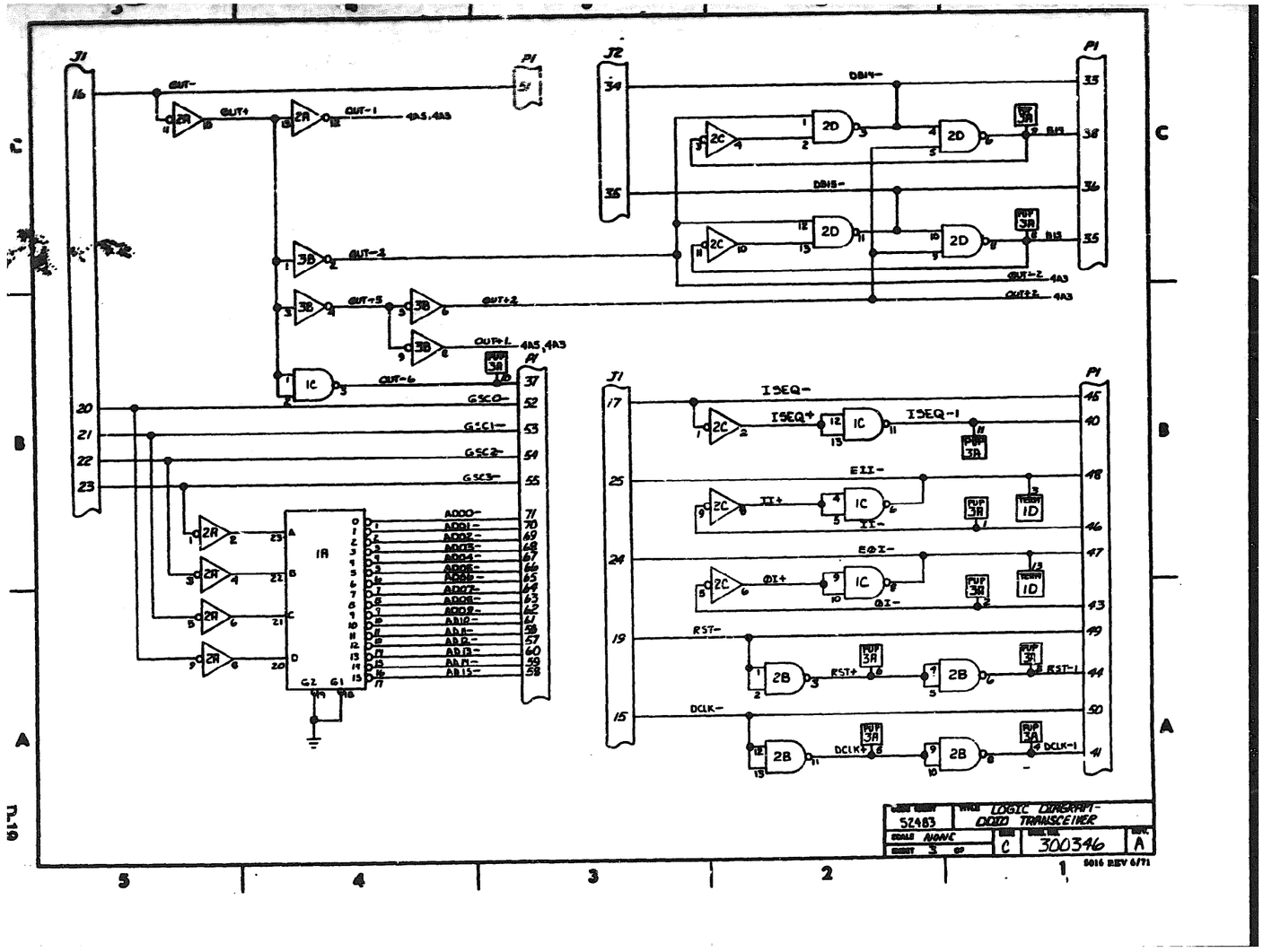


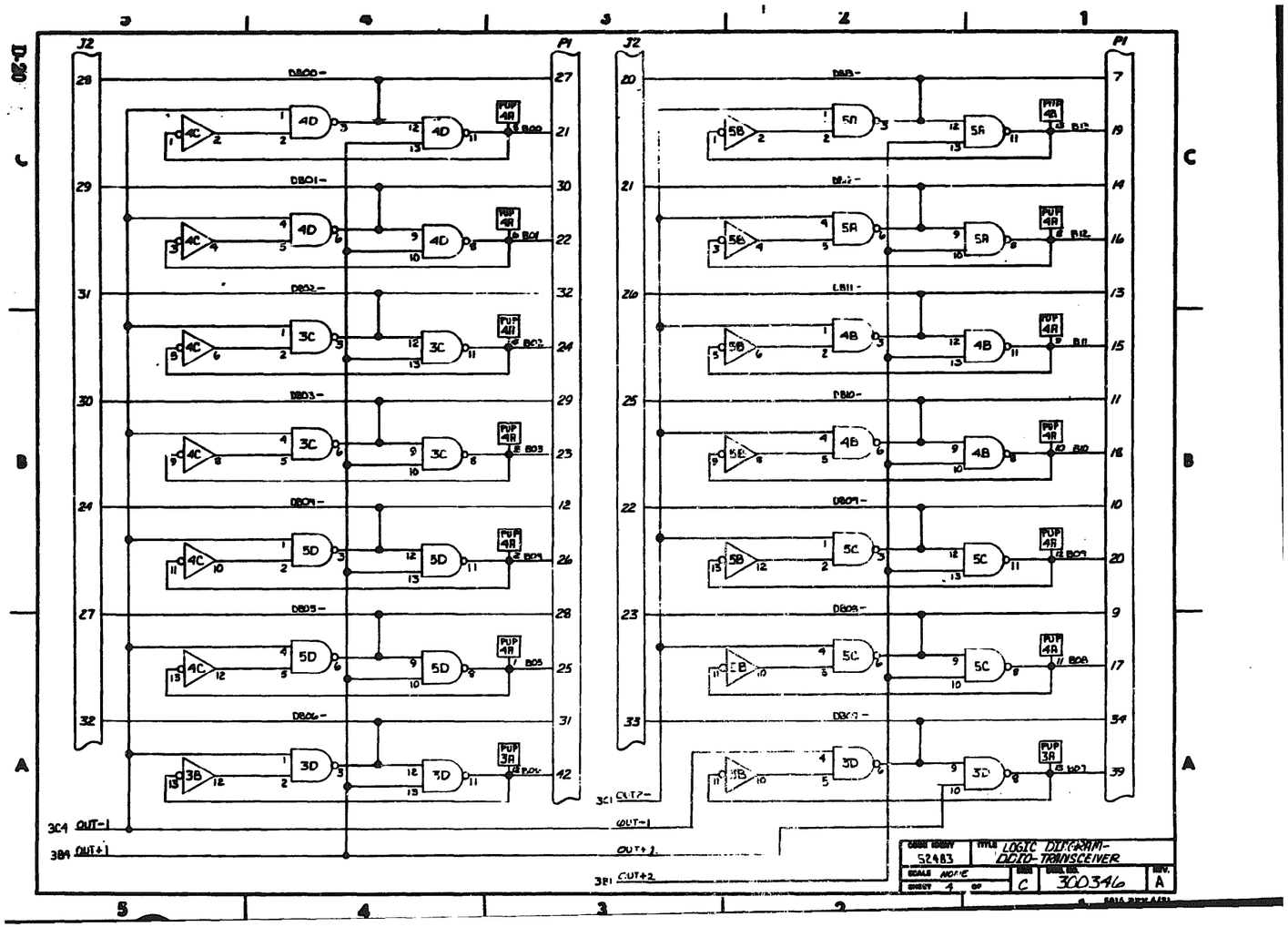
MNEMONIC GLOSSARY

MNEMONIC	SOURCE	DEFINITION
AD(0-15)	3B4,3B4	ADDRESS 0-15
B(0-15)	3B1:4	BUS 0-15
DB(0-15)	3C2:4	DATA BUS
DCLK	3A2	DATA CLOCK
EII	3A2	EXTERNAL INPUT INTERRUPT
EBI	3A2	EXTERNAL OUTPUT INTERRUPT
GSC(0-3)	3A5	GROUP SELECT COUNTER
II	3A2	INPUT INTERRUPT
ISEQ	3A2	INPUT SEQUEANCE
AI	3A2	OUTPUT INTERRUPT
BUT	3A4	OUTPUT TIME
RST	3A2	RESET

	A	B	C	D	
5	800066 7438	800015 74H04	800066 7438	800066 7438	5
4	830096 PUP	800066 7438	800015 74H04	800066 7438	4
3	830096 PUP	800015 74H04	800066 7438	800066 7438	3
2	800015 74H04	800066 7438	800015 74H04	800066 7438	2
1	800060 74154		800066 7438	830095 TERM	1
	A	B	C	D	

CAGE CODE 52483	TITLE LOGIC DIAGRAM - QQIO TRANSCEIVER		
SCALE NONE	SIZE C	DWG. NO. 300346	REV. A
SHEET 2 OF			


J1
P1
J2
OUT-
OUT+
OUT-1
4A5,4A3
OUT-2
OUT+5
OUT+2
OUT+1
OUT-6
DBI4-
DBI5-
BI13
BI15
OUT-2 4A3
OUT+2 4A3
GSC0-
GSC1-
GSC2-
GSC3-
ADDO-
ADD1-
ADD2-
ADD3-
ADD4-
ADD5-
ADD6-
ADD7-
ADD8-
ADD9-
ADD10-
ADD11-
ADD12-
ADD13-
ADD14-
ADD15-
ISEQ-
ISEQ+
ISEQ-1
EII-
II+
II-
EØI-
ØI+
ØI-
RST-
RST+
RST-1
DCLK-
DCLK+
DCLK-1
LOGIC DIAGRAM-
DDD TRANSCEIVER
52483
SCALE NONE
SHEET 3 OF
C
300346
A
5016 REV 6/71


J2
P1
DB00-
DB01-
DB02-
DB03-
DB04-
DB05-
DB06-
3C1 OUT-1
3B1 OUT+1
3C1 OUT+2
3B1 OUT-2
4D
4C
3C
3B
5D
5C
5B
4B
5A
4A
PUP 4R
PUP 4A
PUP 3A
SIZE C
300346
REV. A
5
4
3
2
1
A
B
C
D-20

REV.	E.O. NO.	DATE	DESCRIPTION	DWN	CKD
X1	—	[illegible]	INITIAL RELEASE	S.S.	[illegible]
X2	—	2-1-75	UPDATED SHEET 2	[illegible]	[illegible]
Z	3115	2-4-75	SPECIAL PILOT REL.	[illegible]	[illegible]
A	005279	3-8-75	PRODUCTION RELEASE	S.B	[illegible]

4. ALL SYMBOLS ARE PER GTE/IS DRAFTING STANDARDS MANUAL.

3. ALL CAPACITOR VALUES ARE IN MICROFARADS.

2. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4 W

1. REFERENCE DOCUMENTS:

ASSEMBLY DWG - 104040
TEST SPEC - 250740

SPARE CIRCUITS		
GTE/IS P/N	REF. DES	NO. AVAIL

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C8	
R4	

A	A	A	A													
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

SHEET REVISION STATUS

DWN	S. Snyder	[illegible]
CKD	[illegible]	[illegible]
APP	[illegible]	[illegible]
APP		
APP		
APP	[illegible]	[illegible]

PROPRIETARY INFORMATION

GTE INFORMATION SYSTEMS

CODE IDENT 52483

TITLE LOGIC DIAGRAM - DCIO DIGITAL INPUT BOARD

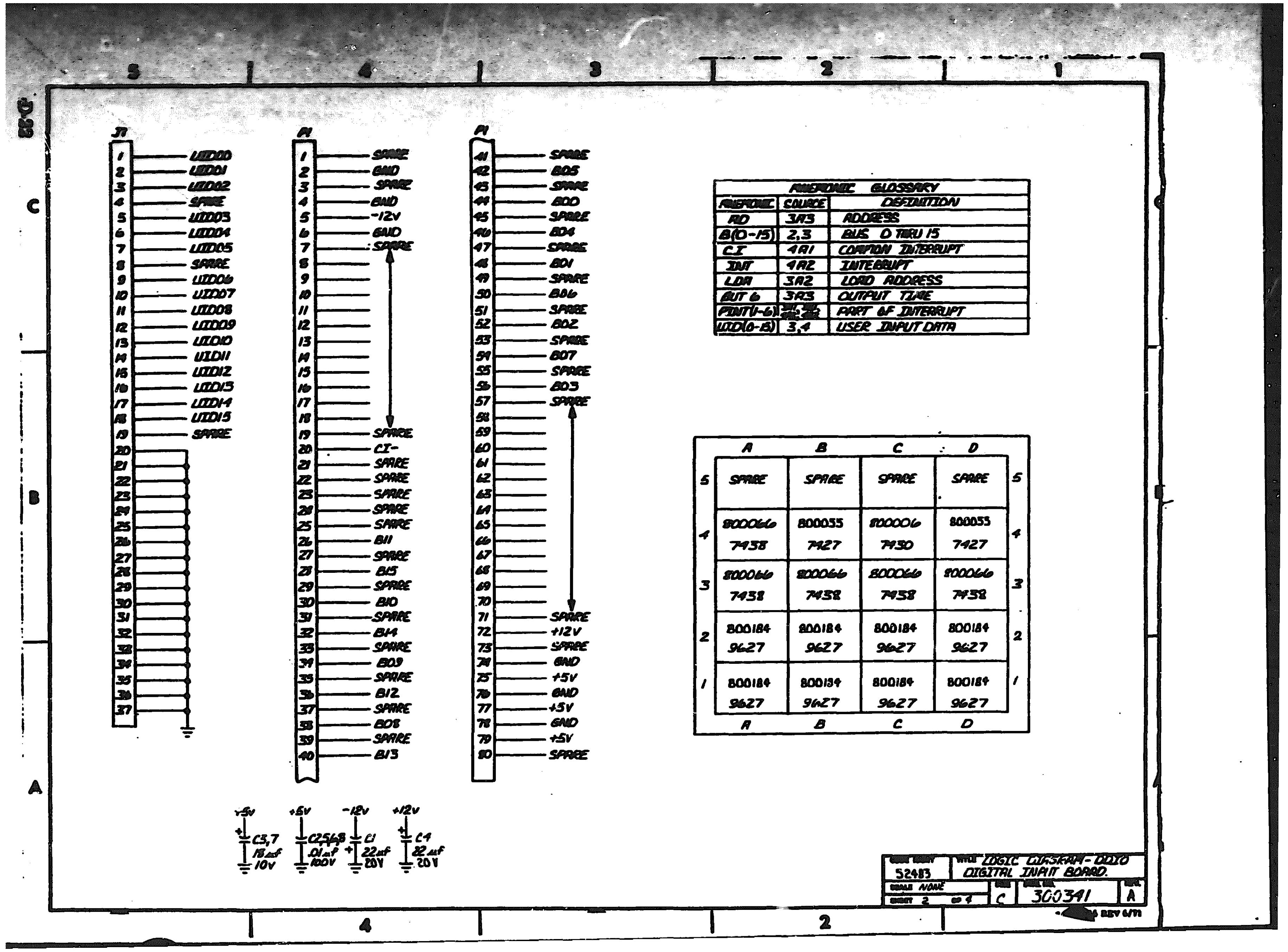
SCALE NONE

SHEET 1 OF 4

SIZE C

DWG. NO. 300341

REV. A


MNEMONIC GLOSSARY
MNEMONIC SOURCE DEFINITION
AD 3A3 ADDRESS
B(0-15) 2,3 BUS 0 THRU 15
CI 4A1 COMMON INTERRUPT
INT 4A2 INTERRUPT
LDA 3A2 LOAD ADDRESS
OUT 6 3A3 OUTPUT TIME
PINT(1-6) PART OF INTERRUPT
UID(0-15) 3,4 USER INPUT DATA
LOGIC DIAGRAM-DDIO
DIGITAL INPUT BOARD
52483
SCALE NONE
SHEET 2 OF 4
C
300341
A

GTE INFORMATION SYSTEMS

ENGINEERING ORDER

E.O. NO. 3824

PRODUCT AFFECTED: 104040

OPER: AN | ECR NO: 3746 | ED TYPE CHNG (K)

DATE 5-18-76 SHT 1 OF 1

E.O. DASH	H	S	D	DOCUMENT – PART NO.	REV. OLD	REV. NEW	TITLE	PER SHT	NEXT ASSEMBLY	DATE INCORP.
			X	300341	A	A1	LOGIC DIA-DDIO DIGITAL INPUT BOARD	-	104040	

PURPOSE

TO CORRECT CONNECTOR DATA ON P1

SPECIFICATIONS

PAGE 2 of 300341

ACTION

CONNECTOR P1 PIN 22 IS 'OUT 6' - WAS 'SPARE'
CONNECTOR P1 PIN 24 IS 'AD-' WAS 'SPARE'

ECP Rel'd DP 5/6/76

COGNIZANT ENGINEER Wm Monroe 5/19/76

COST ANALYSIS REFERENCE: 3746

EFFECT UPON		DESCRIPTION/EFFECTIVITY
FINISHED GOODS	IN FIELD ☐	NA
	IN HOUSE ☐	
WORK IN PROCESS	IN TEST ☐	
	IN PROD. ☐	
PARTS IN STORES ☐		
PARTS ON ORDER ☐		
FIELD RETURNS ☐		
QUALITY CONTROL ☐		
VENDOR TOOLING ☐		NA
DOCUMENTS ☒		AS NOTED
MANUALS ☐		NA

CCB CHAIRMAN DATE 5/19/76

SERVICE CO. DATE 5/19/76

ENGINEERING DATE 5/19/76

MANUFACTURING DATE 5/6/76

QUALITY DATE 5/6/76

RECORDED MD DATE 5/19/76

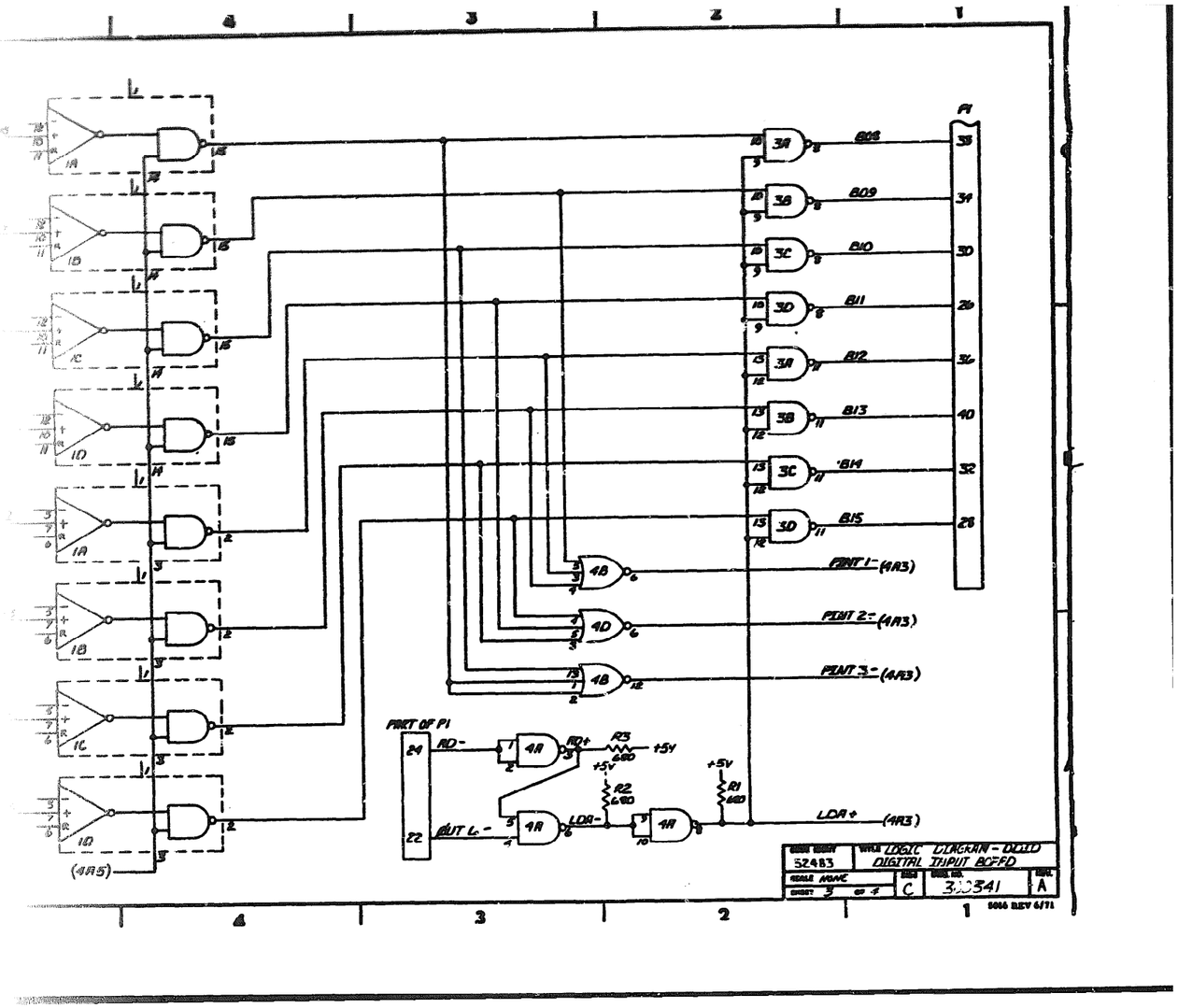
DRAWN MYERS DATE 5-19-76

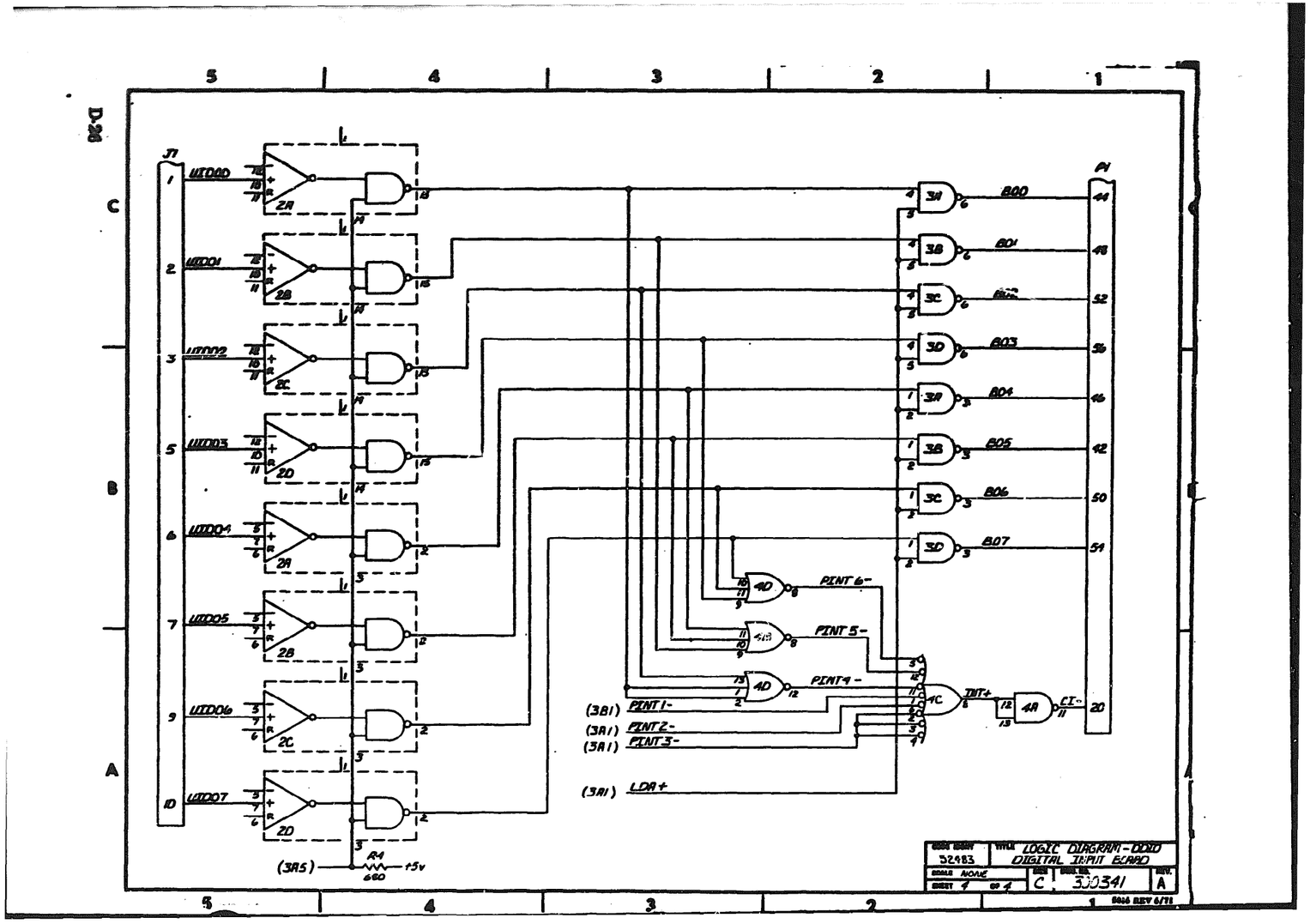
CHECKED MD DATE 5/19/76

RELEASED SC DATE 5-19-76

E.O. NO. 3824

FORM NO. 5025 REV. 1/74


P1
1A
1B
1C
1D
1E
1F
1G
1H
1J
1K
3A
3B
3C
3D
3A
3B
3C
3D
4B
4D
4B
4B
4A
4A
4A
B08
B09
B10
B11
B12
B13
B14
B15
PIN 1 = (4A3)
PIN 2 = (4A3)
PIN 3 = (4A3)
LDR+ (4A3)
PART OF P1
AD-
AD+
OUT L-
LDR-
R3 680
R2 680
R1 680
+5V
(4A5)
LOGIC DIAGRAM - DIGITAL INPUT BOARD
52483
C
30341
A
5006 REV 6/71


5
4
3
2
1
D26
J1
P1
C
B
A
UIDD00
UIDD01
UIDD02
UIDD03
UIDD04
UIDD05
UIDD06
UIDD07
2A
2B
2C
2D
2A
2B
2C
2D
B00
B01
B02
B03
B04
B05
B06
B07
PINT 6-
PINT 5-
PINT 4-
(3B1) PINT 1-
(3A1) PINT 2-
(3A1) PINT 3-
(3A1) LDA+
(3A5)
R4
680
+5v
INT+
CI-
DRAWING NUMBER
52483
TITLE
LOGIC DIAGRAM - D000
DIGITAL INPUT BOARD
SIZE
C
330341
REV.
A

REV	EO. NO.	DATE	DESCRIPTION		
X1	[illegible]	[illegible]	INITIAL RELEASE	S.S.	
X2	[illegible]	1-24-75	[illegible] C13-C44 [illegible]	D.T.	
P	003110	1-24-75	SPECIAL PILOT RELEASE	D.T.	
Z1	003281	5-6-75	[illegible] POLARITY TO C1,2,3,&4	S.B.	
A	003279	5-6-75	PRODUCTION RELEASE	S.B.	

5. CAPACITORS C13-C44 (FOR RISETIME ADJUSTMENT) NOT INSTALLED.
4. ALL SYMBOLS ARE PER GTE.IS DRAFTING STANDARDS MANUAL.
3. ALL CAPACITOR VALUES ARE IN MICROFARADS.
2. ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W.
1. REFERENCE DOCUMENTS:
   ASSEMBLY DWG - 104048
   TEST SPEC - C50740

SPARE CIRCUITS		
GTE/IS P/N	REF.DES.	NO. AVAIL
800179	1C	2
800055	4A	2
800015	4B	3

REFERENCE DESIGNATIONS	
LAST USED	NOT USED
C49	

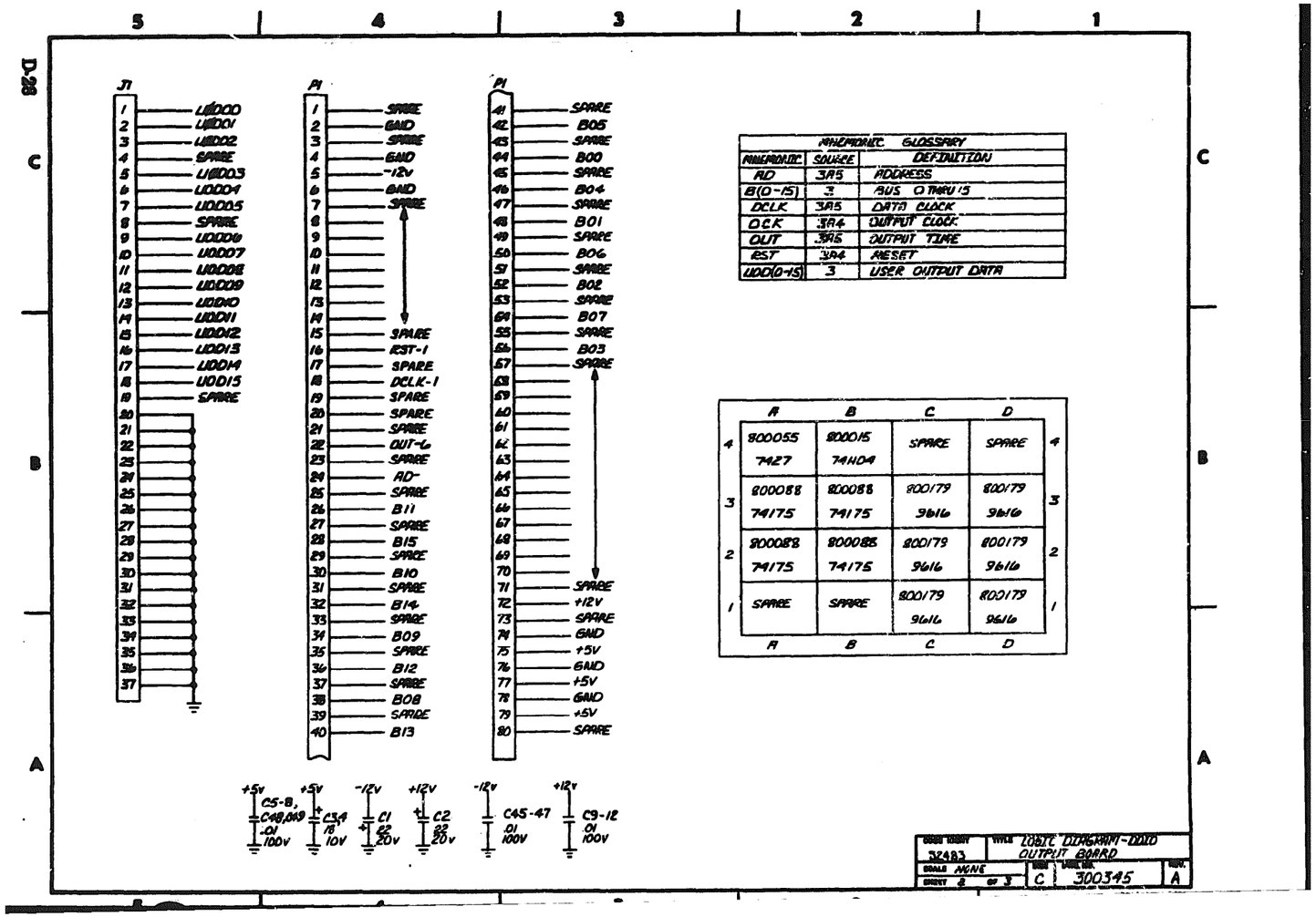
A	A	A
1	2	3

SHEET REVISION STATUS

PROPRIETARY INFORMATION

GTE INFORMATION SYSTEMS

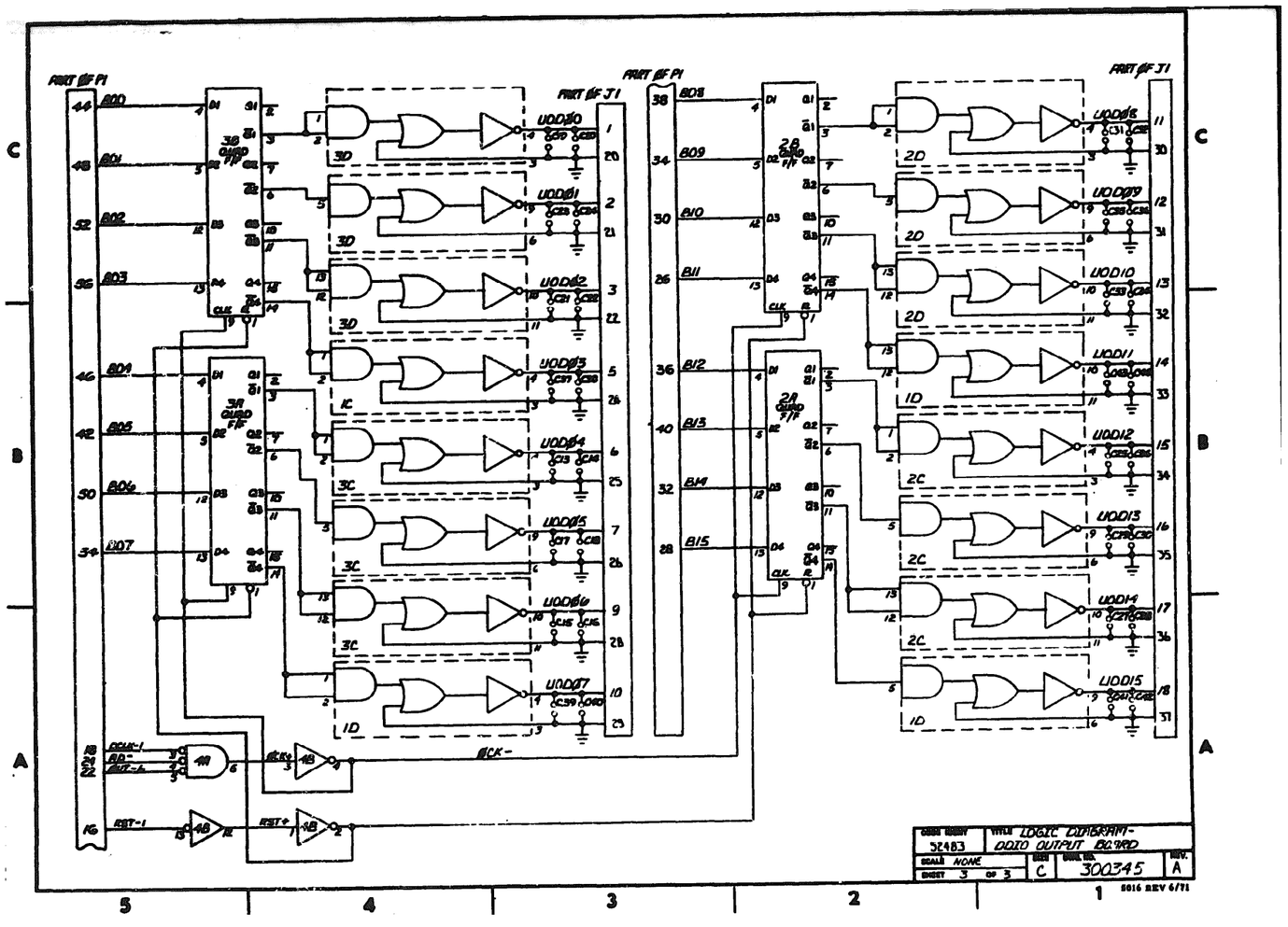
DWN	S. [illegible]
CODE IDENT	52483
TITLE	LOGIC DIAGRAM - DDIO OUTPUT BOARD
SCALE	NONE
SHEET	1 OF 3
SIZE	C
DWG. NO.	300345
REV.	A



MNEMONIC GLOSSARY		
MNEMONIC	SOURCE	DEFINITION
AD	3A5	ADDRESS
B(0-15)	3	BUS 0 THRU 15
DCLK	3A5	DATA CLOCK
OCK	3A4	OUTPUT CLOCK
OUT	3A6	OUTPUT TIME
RST	3A4	RESET
U0D(0-15)	3	USER OUTPUT DATA

	A	B	C	D	
4	800055 7427	800015 74H04	SPARE	SPARE	4
3	800088 74175	800088 74175	800179 9616	800179 9616	3
2	800088 74175	800088 74175	800179 9616	800179 9616	2
1	SPARE	SPARE	800179 9616	800179 9616	1
	A	B	C	D	

ORDER NUMBER 32483	TITLE LOGIC DIAGRAM-U0D OUTPUT BOARD		
SCALE NONE	SIZE C	DRAWING NO. 300345	REV. A
SHEET 2 OF 3			



D-29/(D-30blank)

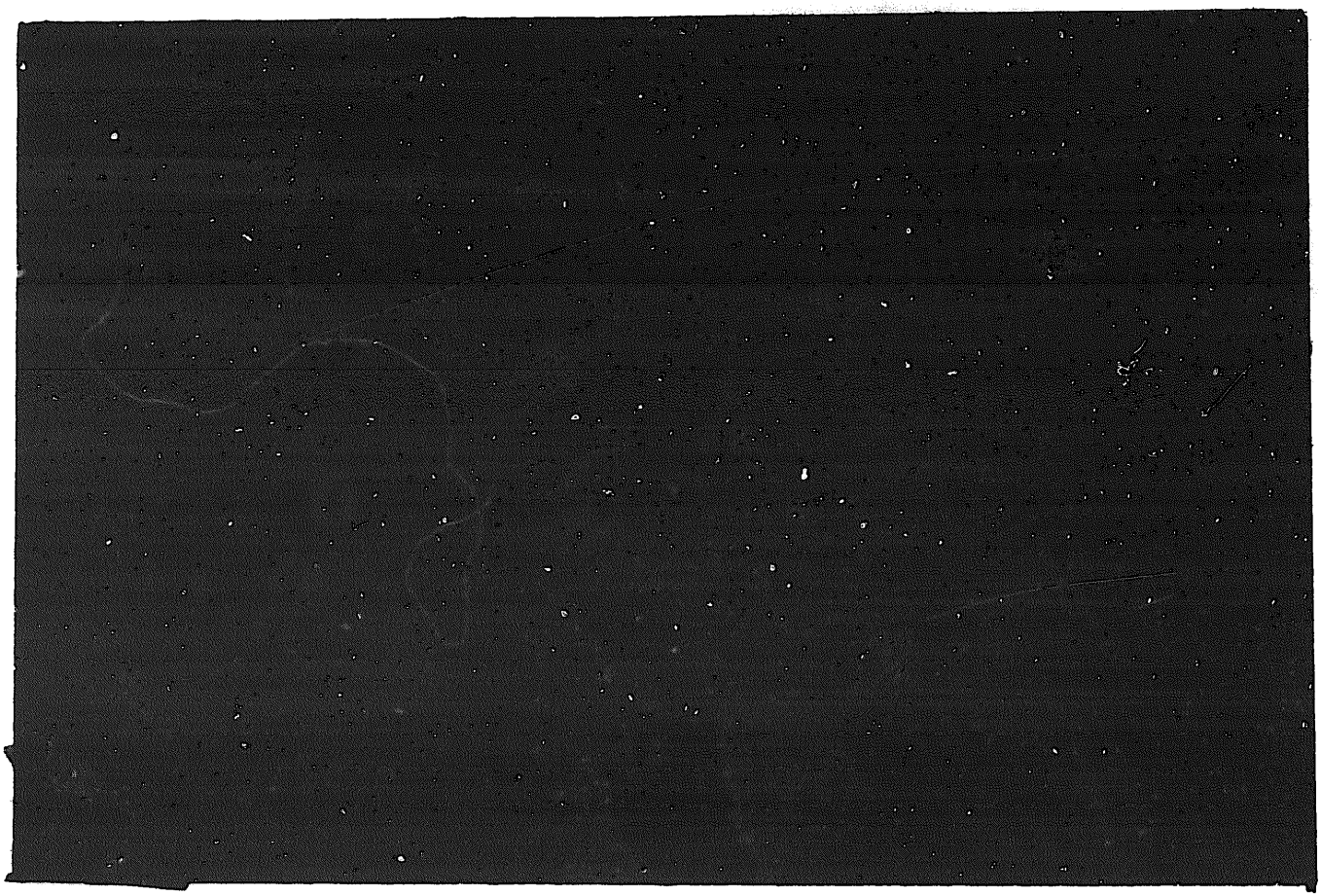
DEPARTMENT OF THE ARMY
US ARMY AG PUBLICATIONS CENTER
1655 WOODSON ROAD
ST. LOUIS, MISSOURI 63114

OFFICIAL BUSINESS
PENALTY FOR PRIVATE USE $300

POSTAGE AND FEES PAID
DEPARTMENT OF THE ARMY
DOD 314

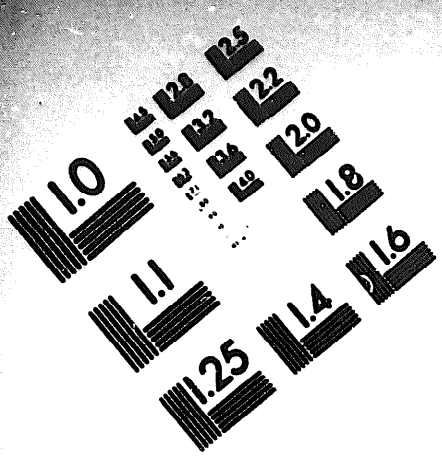
END
03-20-85

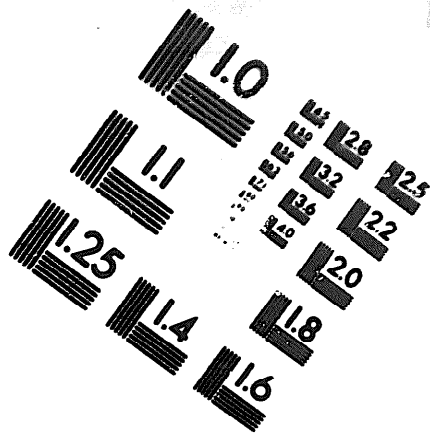
DATE



DEPARTMENT OF THE ARMY

MICROFORM
TEST TARGET





150 MM

1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

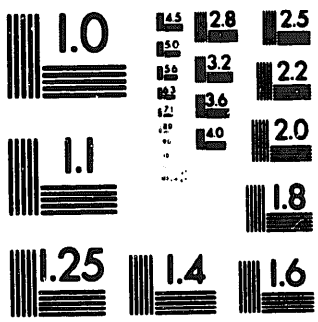
ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*



1.0 mm (e= .81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

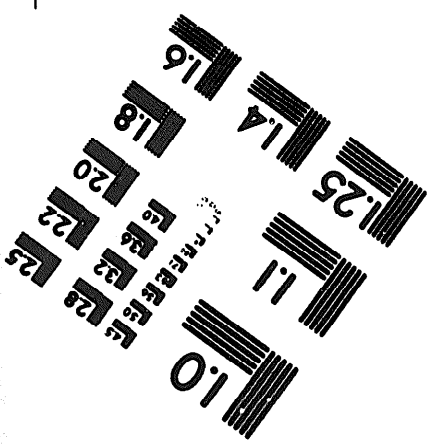
2.0 mm (e= 1.37 mm)

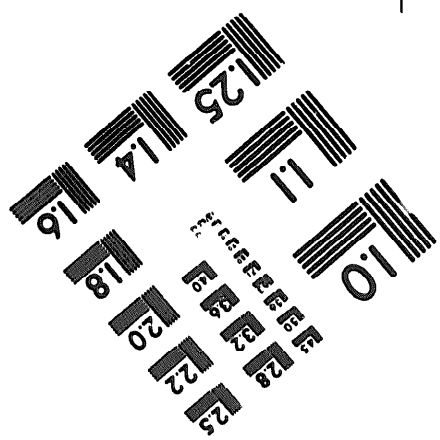
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

200 MM





250 MM